U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

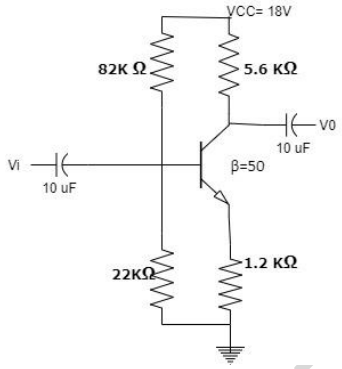
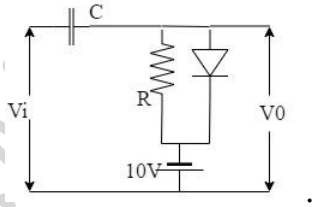
Autonomous Institute Affiliated to VTU

June / July 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 23EC3PCAEC **Max Marks: 100**
Course: Analog Electronic Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Determine the levels of I_{CQ} and V_{CEQ} for the voltage divider bias circuit shown in the figure 1  Figure 1	CO 2	PO 1	6
	b)	Analyze the circuit shown in Figure 2 and sketch the input and ouput voltage waveform assuming an ideal diode. (Vi =20sinωt)  Figure 2	CO3	PO2	06
	c	Draw the r_e model for a voltage divider bias configuration and derive expressions for input impedance, output impedance and voltage gain.	CO2	PO1	08
		OR			
2	a	For the transfer characteristics shown in figure3 identify and analyze the circuit also obtain the output voltage waveform if the input voltage is 50sinwt, (consider ideal diodes)	CO2	PO2	06

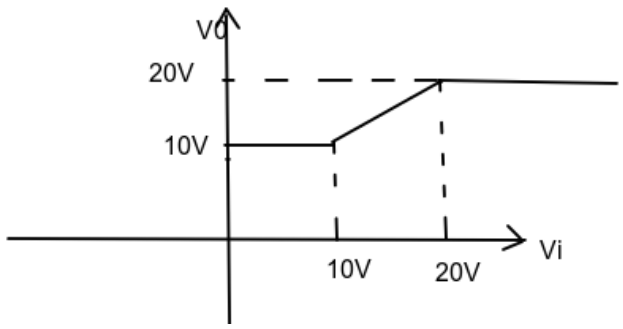
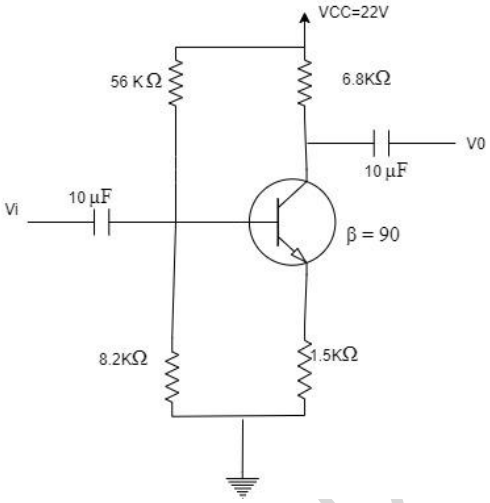
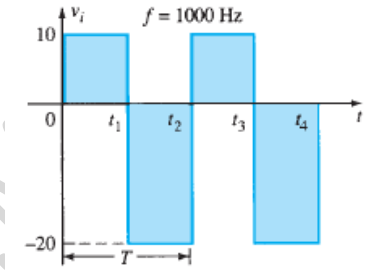
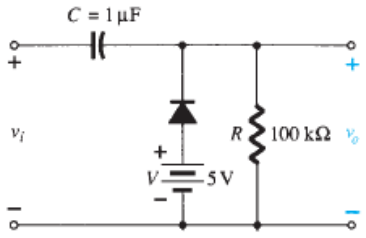
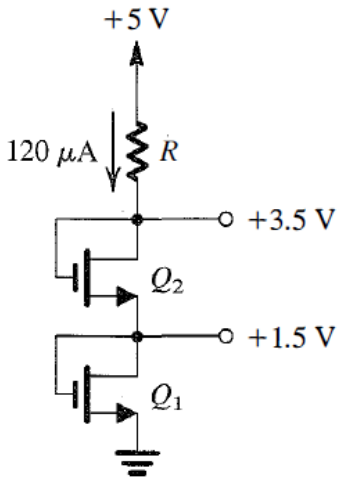
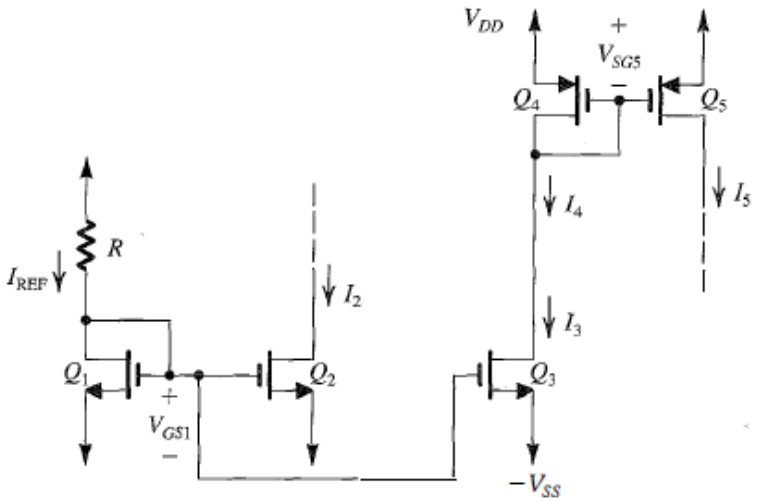


Figure 3

	b	For the circuit shown in the figure 4. determine the following parameters if $r_0 = \infty$ and for r_0 =50KΩ i) re ii) Zi iii)Z0 iv)Av  Figure 4	*CO3*	*PO2*	**10**
	c	Determine output voltage *vo* for the network of Figure. 5 for the input indicated, sketch the input and output voltage waveform.   **Figure 5**	*CO2*	*PO1*	**04**
		UNIT - II			
3	a)	With a neat block diagram derive the expressions for gain with feedback, input impedance and output impedance for current series feedback configuration	*CO2*	*PO1*	**08**
	b)	Calculate gain, input and output admittance for current series feedback amplifier with A= -300, R_i= 1.5KΩ, R_O= 50KΩ and feedback fraction β= -1/15	*CO2*	*PO1*	**06**

		c)	Derive an expression for miller effect induced input and output capacitance for an inverting amplifier	*CO2*	*PO1*	**06**
			UNIT - III			
	4	a)	A class B power amplifier output stage is required to deliver an average power of 100W into a 16 Ω load. The power supply should be 4V greater than the corresponding peak sine-wave output voltage. Determine the power supply voltage required (to the nearest volt in the appropriate direction), the peak current from each supply, the total supply power, and the power conversion efficiency. Also determine the maximum possible power dissipation in each transistor for a sinewave input.	*CO3*	*PO2*	**10**
		b)	With a neat circuit diagram, explain the working of class B push pull power amplifier	*CO1*	-	**06**
		c)	Calculate the total harmonic distortion for an output signal having fundamental amplitude of 2.5V, second harmonic amplitude of 0.25V, third harmonic amplitude of 0.1V and fourth harmonic amplitude of 0.05V.	*CO2*	*PO1*	**04**
			UNIT - IV			
	5	a)	The NMOS transistors in the circuit of Fig. 5 have Vt, == 1 V, $\mu_n C_{ox}$ == 120 μA/v², λ= 0, and L1= L2 = 1 μm. Find the required values of gate width for each of Q1 and Q2, and the value of R, to obtain the voltage and current values indicated.  Figure 5	*CO3*	*PO2*	**10**
		b)	Derive an expression for the drain current of NMOS transistor operating in (i) Triode region and (ii) Saturation region	*CO2*	*PO1*	**10**
			UNIT - V			
	6	a)	Derive an expression for transconductance of the NMOS transistor and show that the transconductance $gm = \frac{2ID}{2Vov}$	*CO2*	*PO1*	**10**
		b)	Derive the terminal parameters for the amplifier circuit which does not produce phase reversal at the output	*CO3*	*PO2*	**10**

			OR			
	7	a)	Derive an expression for i) input impedance ii)output impedance iii)voltage gain and overall voltage gain for a common source amplifier with source resistance	*CO2*	*PO1*	**10**
		b)	Identify the circuit shown in the figure 9, explain its significance in biasing the MOS amplifier  Figure 9	*CO3*	*PO2*	**10**

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