U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

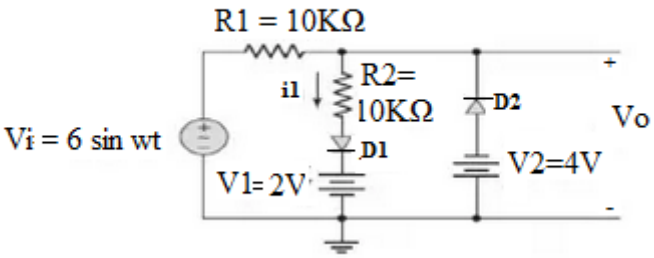
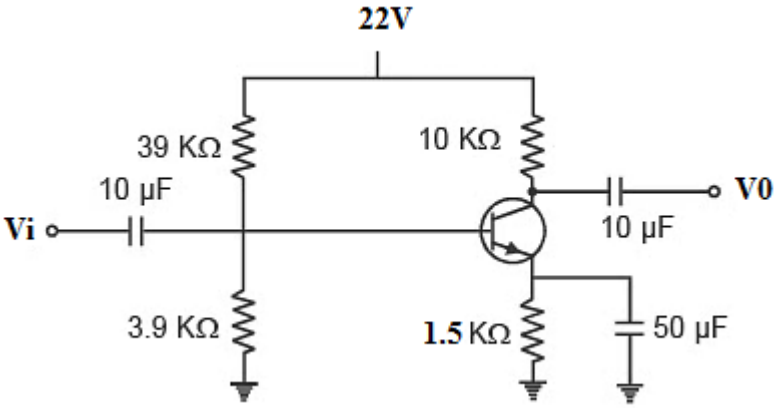
Autonomous Institute Affiliated to VTU

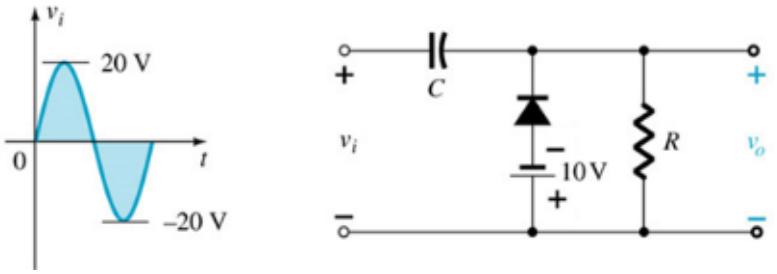
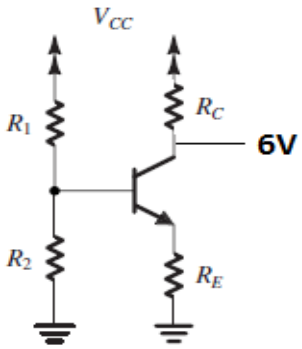
April 2024 Semester End Main Examinations

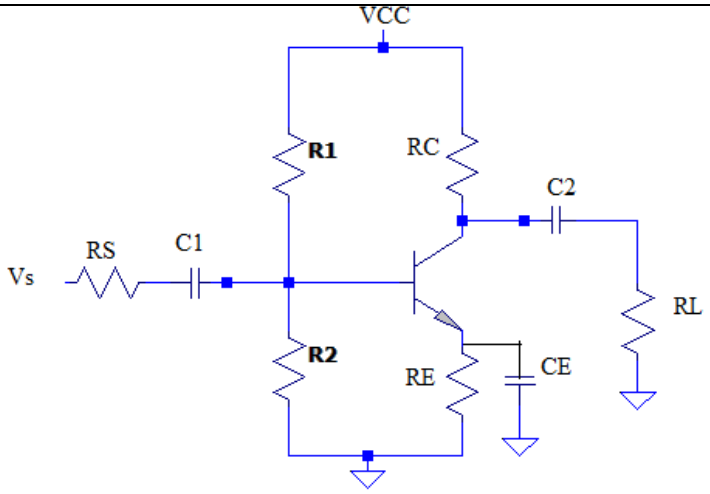
Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 23EC3PCAEC **Max Marks: 100**
Course: Analog Electronic Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Find the output of the parallel based clipper shown in Fig 1a. Assume Vγ and rf=0 for the diodes. Illustrate the same with input and output waveforms.  Fig 1a	CO2	PO 1	**06**
	b)		Determine the operating point (V_{CE}, Ic) for the circuit shown in Fig 1b. Assume β of the transistor to be 140.  Fig 1b	CO 2	PO1	**06**
	c)		For a common emitter amplifier draw re model and derive expressions for voltage gain, input impedance, output impedance and current gain.	CO 2	PO1	**08**
			OR			

	2	a)	Determine the current gain, input impedance and voltage gain for a common emitter configuration with a load impedance of 2KΩ. Assume that the npn transistor used has β=120 and emitter current of 3.2mA. Let r_0=∞Ω.	*CO 2*	*PO1*	**06**
		b)	Consider the clamping circuit shown in Fig 2b and plot the output waveform. Assume the diode is ideal.  Fig 2b	*CO 2*	*PO1*	**06**
		c)	Design the bias network of the amplifier shown in Fig. 2c to establish a current I_E = 1 mA using a power supply V_{CC} = +12 V. The transistor is specified to have a nominal β = 100. Allocate one-third of the supply voltage to the voltage drop across R_2 and I_E=1mA.  Fig 2c	*CO 4*	*PO3*	**08**
			UNIT - II			
	3	a)	Determine the Voltage gain V_0/V_i, V_0/V_s and lower cutoff frequency for the circuit shown in Fig 3a. Assume C_1= 10μF, C_E= 20 μF, C_2= 1 μF, Rs= 1KΩ, R_1= 40 KΩ, R_2=10 KΩ, R_E=2 KΩ, R_C=4 KΩ, R_L=2.2 KΩ, β=100, Vcc=20V, r_0=∞Ω.	*CO 2*	*PO1*	**10**

			 Fig 3a			
	b)	An amplifier has a gain A, input impedance Ri and output impedance R_0. Derive the expression for input and output impedance when a voltage series negative feedback is provided to the amplifier with a feedback factor β.	*CO 2*	*PO1*	**10**
		UNIT - III			
4	a)	For a series fed class A power amplifier prove that maximum efficiency if 25%.	*CO 2*	*PO1*	**06**
	b)	For a class B amplifier using a supply of V_{CC}=30V and driving a load of 16Ω, find the maximum input power, output power and transistor dissipation.	*CO 2*	*PO1*	**06**
	c)	Analyse the working of a transformer coupled class B power amplifier and also the drawbacks of the same.	*CO 3*	*PO2*	**08**
		UNIT - IV			
5	a)	With suitable figures deduce Id- V_{DS} relationship in linear and in saturation region	*CO 2*	*PO1*	**10**
	b)	With neat sketches explain the device structure and operation of NMOSFET for various conditions of V_{GS} and V_{DS}.	*CO 2*	*PO1*	**10**
		UNIT - V			
6	a)	Analyse the working of a common source amplifier with degeneration resistance and arrive at the expressions for voltage gain and output impedance of the amplifier.	*CO 3*	*PO2*	**10**
	b)	Derive an expression for output impedance of Wilson mirror using MOSFETS	*CO 2*	*PO1*	**10**
		OR			
7	a)	Analyse a Common Gate amplifier with resistive load. Obtain the expression for small signal voltage gain. Draw the small signal equivalent circuit and obtain the expressions.	*CO 3*	*PO2*	**10**
	b)	Deduce relevant expression for voltage gain of a source follower with a small signal model.	*CO 2*	*PO1*	**10**

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