U.S.N.										

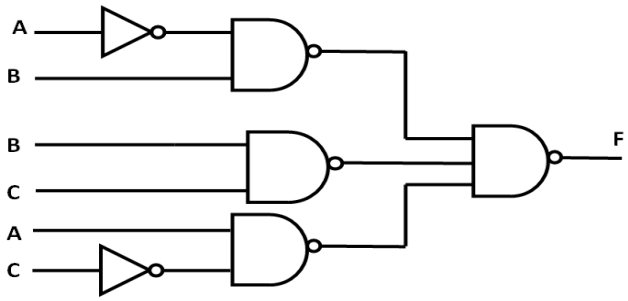
B.M.S. College of Engineering, Bengaluru-560019

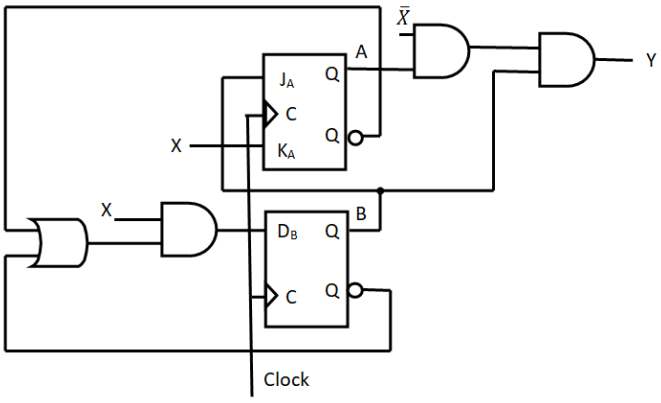
Autonomous Institute Affiliated to VTU

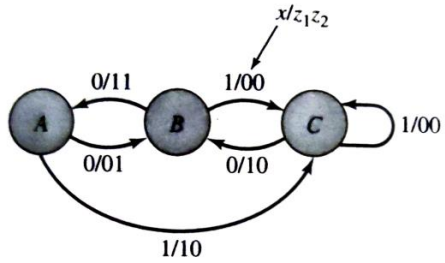
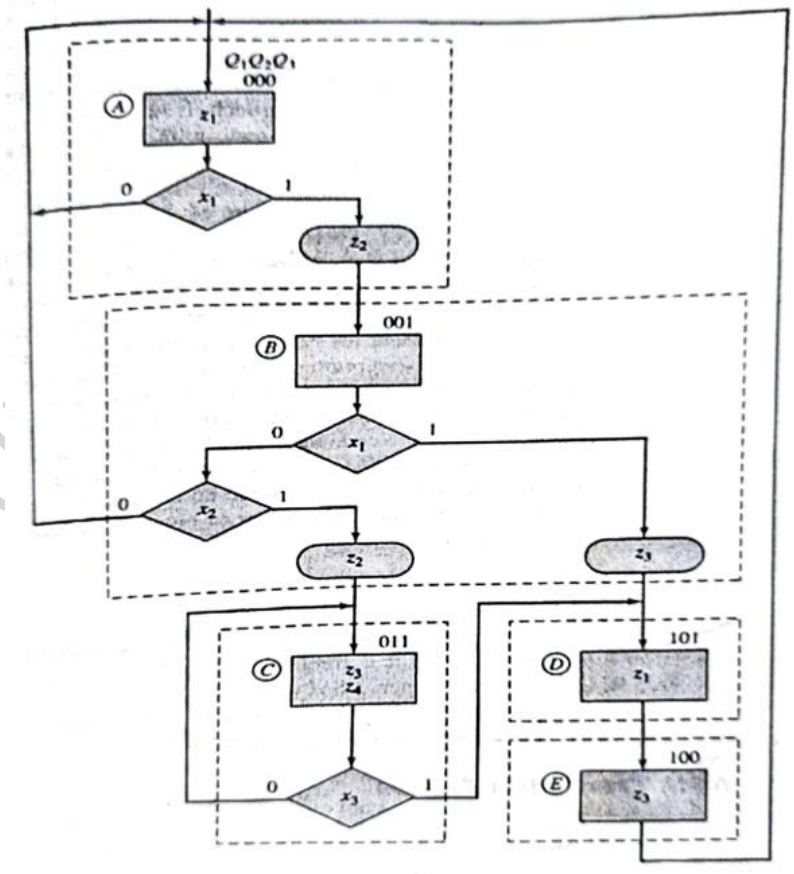
October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 23EC3PCDCD **Max Marks: 100**
Course: Digital Circuit Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

		UNIT - I	CO	PO	Marks
1	a)	Given the Boolean expression $F = m_0 + m_1 + m_2 + m_3 + m_5 + m_7 + m_8 + m_{10}$ where all m_x are the minterms to the input variables P,Q,R and S, find the simplified SOP expression for F and realize using NAND gates.	*CO 1*	*PO 1*	**08**
	b)	In a combinational circuit of 4 variables A,B,C and D, the output is equal to 1 if input variables have more 0's than 1's. The output is zero otherwise. Derive the expression and write the circuit with basic logic gates for the same.	*CO 1*	*PO 1*	**08**
	c)	Analyze the below logical circuit and find simplified output expression using Boolean laws. 	*CO 2*	*PO 2*	**04**
		UNIT - II			
2	a)	Design a combinational circuit to implement the following Boolean function $f(a,b,c,d) = \sum m(0,1,5,6,7,9,10,15)$ using i) 8X1 Multiplexer with a,b,c as select lines ii) 4:16 decoder with active low output	*CO 3*	*PO 3*	**08**
	b)	Implement the following using 3X4X2 PLA with both true and complemented outputs	*CO 1*	*PO 1*	**06**

			$f_1(a,b,c) = \sum m(0,1,3,5)$ $f_2(a,b,c) = \sum m(0,2,3,4)$			
		c)	Design a BCD adder using 4-bit parallel adders by drawing its logical circuit	***CO 3***	***PO 3***	**06**
			UNIT III			
	3	a)	Explain the working of positive edge triggered D flip-flop with timing diagram	-	-	**06**
		b)	Convert JK flip-flop to AB flip-flop. Function table of AB flip-flop is described in the below table **A** | **B** | **Q(t+1)** 0 | 0 | 0 0 | 1 | Q' 1 | 0 | Q 1 | 1 | 1	***CO 1***	***PO 1***	**07**
		c)	Design Mod-6 asynchronous down counter using positive edge triggered JK flip-flop with initial state as '111'. Draw the timing diagram	***CO 3***	***PO 3***	**07**
			OR			
	4	a)	Briefly explain the race around condition in JK flip-flop. What are the ways of eliminating this condition?	-	-	**06**
		b)	Design a 4-bit shift register to perform the following operations Select Lines: S1, S0 | Register Operations 0 0 | Hold 0 1 | Synchronous clear 1 0 | Complement the content 1 1 | Circular shift right	***CO 3***	***PO 3***	**07**
		c)	Design Mod-6 synchronous counter to count the sequence 0-2-3-6-5-1-0 using D flip-flop.	***CO 3***	***PO 3***	**07**
			UNIT IV			
	5	a)	Analyze the synchronous sequential circuit shown in the figure. Obtain the state table and state diagram. Identify the machine 	***CO 2***	***PO 2***	**08**
		b)	Draw the Mealy and Moore state diagram to detect the sequence "101"	***CO 1***	***PO 1***	**06**

		c)	Design a circuit with Mealy network to implement serial binary adder	*CO 3*	*PO 3*	**06**
			UNIT - V			
	6	a)	What are the basic components of ASM charts? Discuss the role of each with proper notation and design an ASM chart for the sequence recognizer to search for X_1X_2 = 01,01,11,00.	*CO 1*	*PO 1*	**10**
		b)	Design ASM chart for binary multiplier write ASM transition and assigned ASM transition tables.	*CO 3*	*PO 3*	**10**
			OR			
	7	a)	Explain parallel and serial decision boxes with an example.	-	-	**6**
		b)	Develop an ASM chart for the below state diagram.  	*CO2*	*PO2*	**4**
		c)	Analyze the ASM chart given below and realize with discrete gates and clocked d flip-flop.  	*CO 2*	*PO 2*	**10**

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