U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

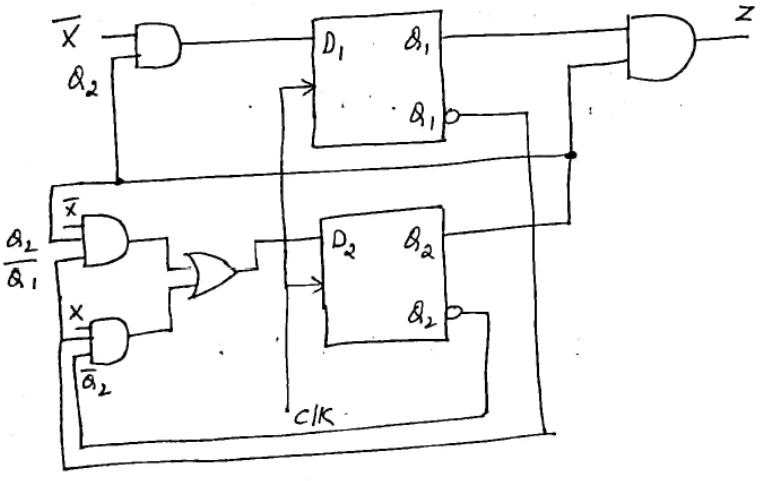
Course Code: 23EC3PCDCD **Max Marks: 100**

Course: Digital Circuit Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Express the function i) $T = r(\bar{q} + s)(\bar{r} + \bar{q})$ into Maxterm canonical form ii) $Y = \bar{a}\,bc + c\bar{d} + ac\bar{d}$ into Minterm canonical form	CO 1	PO 1	10
	b)	Determine minimal sum and minimal product using K-map f(a, b, c, d) =∑m(1,2,3,4,9,10)+dc(0,14,15)	CO 1	PO 1	10
		OR			
2	a)	Given the logical equation Y= ab + (a'+ b') c + ab i) Simplify and realize the equation using NAND gates only ii) Express the function as Standard SOP and Standard POS form iii)Express the function as prime implicants and prime implicates	CO 1	PO 1	6
	b)	Construct a combinational circuit that has 4-input and 1-output, indicates when numbers are divisible by 2 or 7.	CO 1	PO 1	8
	c)	Obtain minimal SOP expression using K-Map and realize the simplified expression using NAND gates only. f(w, x, y, z) = π M(0,2,3,7, 8,9,10)	CO 1	PO 1	6
		UNIT - II			
3	a)	Illustrate the functionality of Carry Look Ahead Adder	CO 1	PO 1	10
	b)	Design Half Adder and Half Subtractor using 4:1 Mux.	CO 3	PO 3	6
	c)	Explain working of priority Encoder with necessary diagrams.	CO 1	PO 1	4
		OR			
4	a)	Realize Binary full adder and full Subtractor using 2:4 Decoder and NAND gate	CO1	PO 1	8
	b)	Illustrate how PLA can be used for combinational logic design with reference to the functions. Assume 3X4X2 PLA is available. $f_1(X,Y,Z) = \sum m(0,1,3,4)$ $f_2(X,Y,Z) = \sum m(1,2,3,4,5)$.	CO 3	PO 3	6

		c)	Illustrate the functionality of ROM and PLA	*CO 1*	*PO 1*	**6**
			UNIT - III			
	5	a)	What is Race around condition? Explain how it is eliminated by using Master Slave JK Flip flop. Analyze your solution with appropriate logic diagrams. Also draw the waveforms.	*CO 1*	*PO 1*	**10**
		b)	Design a synchronous counter using JK Flip-flop to count the sequence 0-5-3-4-1-6-0 by obtaining minimal sum equations.	*CO 3*	*PO 3*	**10**
			OR			
	6	a)	Design and explain a 4 bit shift register using positive edge triggered D FF to operate as indicated in the table. Mode Control S1 S0 / Operation 0 0 — Hold 0 1 — Shift Right 1 0 — Shift Left 1 1 — Parallel Operation	*CO 3*	*PO 3*	**10**
		b)	Construct Mod 6 Synchronous Up Counter using J K Flip-flop with necessary tables and waveforms.	*CO 1*	*PO 1*	**10**
			UNIT - IV			
	7	a)	Analyze the sequential circuit given in Fig.7a  Fig. 7a	*CO 2*	*PO 2*	**10**
		b)	Design a synchronous circuit using positive edge triggered T-flip-flop to generate the following sequence 0-1-3-0 if input X=0 and 0-3-2-0 if input X=1. Provide an output to go high to indicate non-zero states irrespective of the sequence.	*CO 3*	*PO 3*	**10**

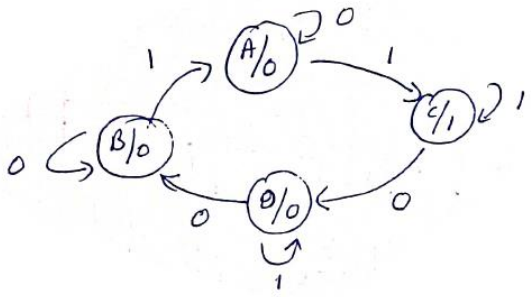
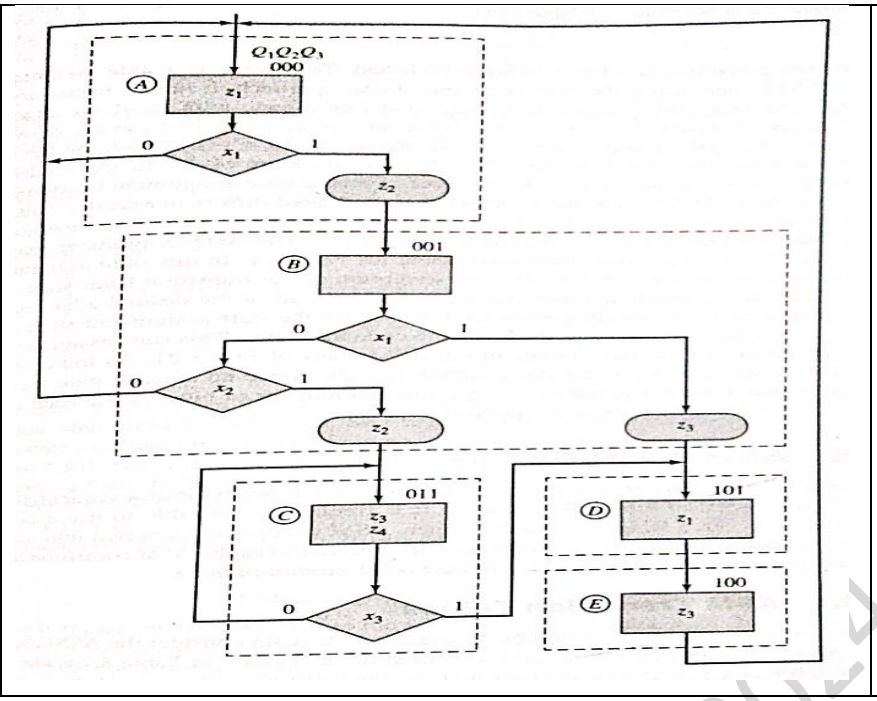
<table>
<tr><td></td><td></td><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td></td><td>8</td><td>a)</td><td>Analyse the state graph given in Fig 8a and realize the circuit using JK FF.
 

Fig. 8a</td><td>CO 2</td><td>PO 2</td><td>10</td></tr>
<tr><td></td><td></td><td>b)</td><td>Derive the State equations for the sequential circuit specified by the following state table. Design the circuit using JK Flip-flop.
<table>
<tr><th>Present State</th><th colspan="2">Next State</th><th colspan="2">Output</th></tr>
<tr><th></th><th>X=0</th><th>X=1</th><th>X=0</th><th>X=1</th></tr>
<tr><td>0 0</td><td>01</td><td>00</td><td>0</td><td>1</td></tr>
<tr><td>0 1</td><td>10</td><td>11</td><td>1</td><td>0</td></tr>
<tr><td>1 0</td><td>00</td><td>01</td><td>1</td><td>0</td></tr>
<tr><td>1 1</td><td>11</td><td>10</td><td>0</td><td>1</td></tr>
</table></td><td>CO 3</td><td>PO 3</td><td>10</td></tr>
<tr><td></td><td></td><td></td><td>UNIT - V</td><td></td><td></td><td></td></tr>
<tr><td></td><td>9</td><td>a)</td><td>Draw state diagram for Mealy state machine to detect sequence "1010" and also construct ASM chart for the same.</td><td>CO 2</td><td>PO 2</td><td>10</td></tr>
<tr><td></td><td></td><td>b)</td><td>Design an ASM chart for binary multiplier</td><td>CO 3</td><td>PO 3</td><td>10</td></tr>
<tr><td></td><td></td><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td></td><td>10</td><td>a)</td><td>Construct an ASM chart for a synchronous sequential network that is to recognize the input sequence of pairs x1 x2=01,01,11,00. Output z is to be 1 when x1x2=00.</td><td>CO 2</td><td>PO 2</td><td>10</td></tr>
<tr><td></td><td></td><td>b)</td><td>Design circuit using D-flip flop for the given ASM chart.</td><td>CO 3</td><td>PO 3</td><td>10</td></tr>
</table>

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