U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

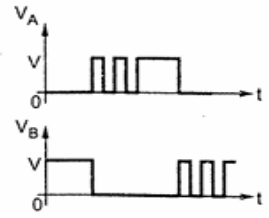
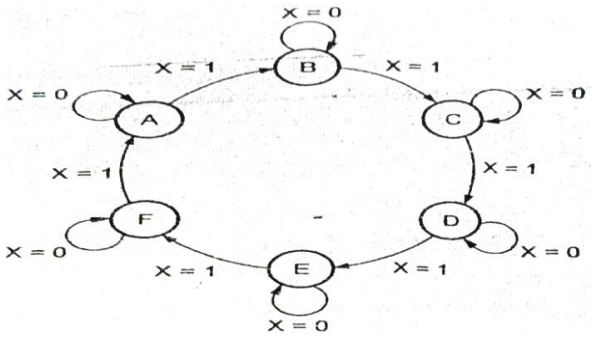
April 2024 Semester End Main Examinations

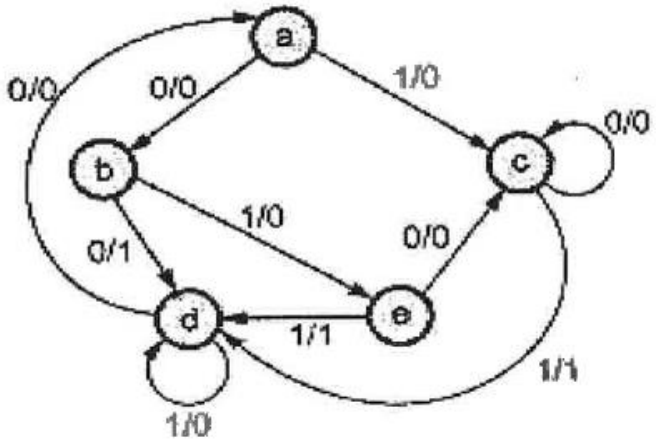
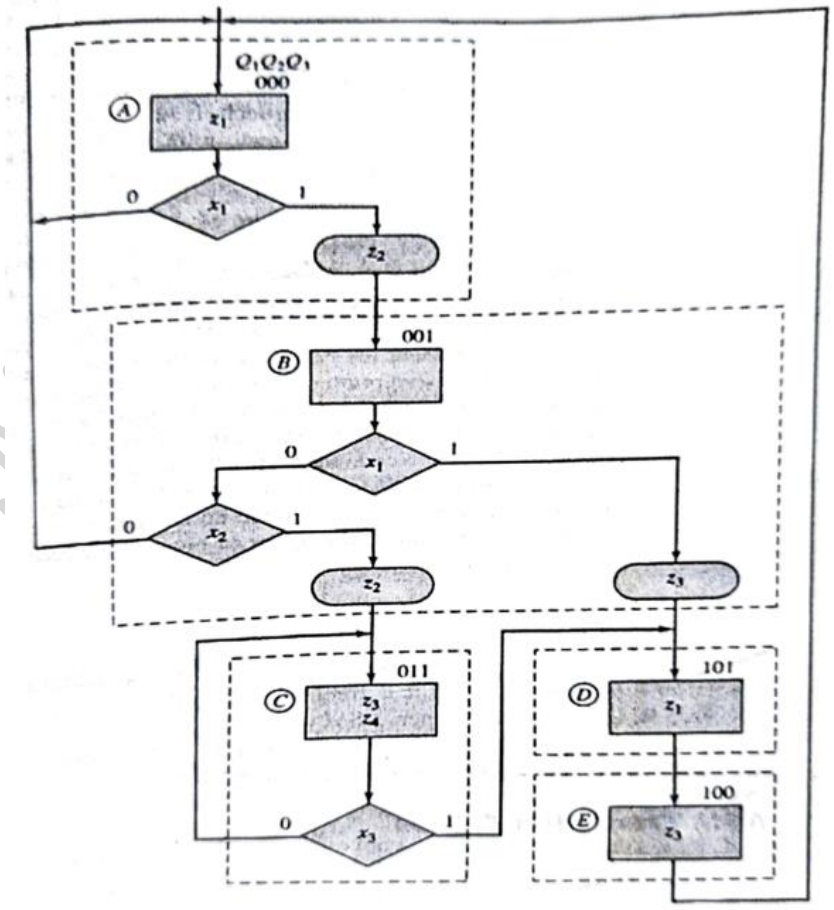
Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 23EC3PCDCD **Max Marks: 100**
Course: Digital Circuit Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Simplify the following Boolean function using K-map and implement. (i) $F_1(a,b,c,d)=\Sigma m(1,3,4,5,13,15)+\Sigma d(8,9,10,11)$ using NAND gates only. (ii) $F_2(a,b,c,d)= \Pi M(0,3,4,7,8,10,12,14)+d(2,6)$ using NOR gates only.	*CO1*	*PO1*	**8**
	b)	In a simple copy machine, a stop signal, S, is to be generated to stop the machine operation and energize an indicator light whenever either of the following conditions exists: (1) there is no paper in the paper feeder tray; or (2) the two microswitches in the paper path are activated, indicating a jam in the paper path. The presence of paper in the feeder tray is indicated by a HIGH at logic signal P. Each of the microswitches produces a logic signal (Q and R) that goes HIGH whenever paper is passing over the switch to activate it. Design the logic circuit to produce a HIGH at output signal S for the stated conditions.	*CO 3*	*PO 3*	**7**
	c)	Determine the prime implicants and essential prime implicants for the given function f(A,B,C,D) = $\sum(0,2,3,5,7,8,9,10,11,13,15)$	*CO 1*	*PO 1*	**5**
		UNIT - II			
2	a)	Implement Y= $\overline{A}\,\overline{D} + B\,\overline{D} + \overline{B}\,\overline{C}\,D$ using 4:1 MUX using AB as a select line inputs.	*CO 1*	*PO 1*	**7**
	b)	Design a 8-bit Magnitude using two 4-bit comparators and logic gates.	*CO 3*	*PO 3*	**7**
	c)	Implement the following Boolean functions using 3x4x2 PLA also write the PLA table. F1(a,b,c)= $\Sigma(0,1,3,4)$ F2(a,b,c)= $\Sigma(1,2,3,4,5)$	*CO 1*	*PO 1*	**6**

			UNIT - III			
	3	a)	Analyze the problem associated with the below timing diagram and explain how it can be avoided with a proper circuit and provide the correct timing diagram.  	***CO 2***	***PO 2***	**6**
		b)	Realize JK flipflop from SR flip flop.	***CO 1***	***PO 1***	**6**
		c)	Design a MOD-6 asynchronous ripple counter using T flipflops.	***CO 3***	***PO 3***	**8**
			OR			
	4	a)	Derive the characteristic equation of D, SR, T and JK flip flops.	***CO 1***	***PO 1***	**8**
		b)	Design a 4-bit universal shift register using D flipflops and MUX with mode selection inputs S1 and S0. The register operates as follows: S1 | S0 | Register Operation 0 | 0 | No change 0 | 1 | Complement 1 | 0 | Clear to 0 1 | 1 | Load parallel data	***CO 3***	***PO 3***	**4**
		c)	Using negative edge triggered SR flip flops, design a counter which counts in the following Sequence: 000,111,110,101,100,011,010,001,000…	***CO 3***	***PO 3***	**8**
			UNIT – IV			
	5	a)	Design a counter for the given state diagram below, using D-Flip Flops. Assume state assignment as A=000, B=010, C=011, D=101, E=110 and F=111.  	***CO 3***	***PO 3***	**8**
		b)	Design a Moore type sequence detector using D-flip flops to detect sequence 1101. Consider the non-overlapping case.	***CO 3***	***PO 3***	**8**
		c)	Analyze the below given state diagram and write the reduced state diagram.	***CO 2***	***PO 2***	**4**

						
			UNIT - V			
6	a)	Design an ASM chart to recognize the sequence X_1X_2=01,01,11,00.		***CO 3***	***PO 3***	**6**
	b)	Develop a ASM chart, if there is one input or control line C, if C=1 it works as up counter otherwise as a down counter. If it reaches to maximum value output turns to be high otherwise low.		***CO 3***	***PO 3***	**6**
	c)	Design a PLA with clocked D-flipflop for the ASM Chart given 		***CO 3***	***PO 3***	**8**

			OR			
	7	a)	Draw state diagram for Mealy state machine to detect sequence "1010" and also construct ASM chart for the same.	***CO 1***	***PO 1***	**8**
		b)	Develop the ASM chart for the following state machine: A two bit up counter with output Q_1Q_0 and enable signal 'X' is to be designed. IF 'X=0, counter changes the state as 00-01-10-11-00. If X=1, counter should remain in present state. Design a circuit using JK-flipflop and a suitable MUX.	***CO 3***	***PO 3***	**12**

****