U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 23EC3PCDCD **Max Marks: 100**

Course: Digital Circuit Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

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Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Simplify the following in the respective canonical forms using Boolean laws (i) F_1=a+ab+a$\bar{c}$d into minterms (ii) F2=a(b+c)(a+c+$\bar{d}$) into maxterms	CO1	PO 1	6
	b)		Determine prime implicant and essential prime implicant for the given function F(a,b,c,d)=πM(0,1,4,5,8,9,11)+d(2,10). Simplify the given function using K-map and realize using logic gates	CO 1	PO 1	7
	c)		Simplify the following expression using Karnaugh map. F(a,b,c,d)=π(0,3,4,7,8,10,12,14)+∑d(2,6). Design the simplified expression using only NOR gates.	CO 1	PO 1	7
			OR			
2	a)		In a copy machine, a stop signal(S) to be generated to stop the machine operation and energize an indicator light whenever either of the following conditions exists: (1) There is no paper in the paper feeder tray (signal P) or (2) The both the microswitches (Q and R) in the paper path are activated, indicating a jam in the paper path. The presence of paper in the feeder tray is indicated by a HIGH at logic signal P. Each of the microswitches (Q and R) produces a logic signal that goes HIGH one after other whenever paper is passing over the switches. Design the logic circuit to produce a HIGH at output signal S for the stated conditions.	CO 1	PO 1	8
	b)		Simplify the following function in SOP form using K-map F(A,B,C,D)= AD + $\overline{A}\,\overline{B}\,C + B\overline{D} + C\overline{D} + A\overline{C}$	CO 1	PO 1	6
	c)		Express the following Boolean function into their proper canonical form (i) M=p($\overline{q}$ +s) (ii) N=$(\overline{w}+x)(y+z)$	CO 1	PO 1	6

			UNIT - II			
	3	a)	Design a 4-bit parallel adder with look ahead carry generator.	***CO 3***	***PO 3***	**7**
		b)	Design 3-bit gray to binary converter using 3-to-8-line decoder with active high outputs.	***CO 3***	***PO 3***	**5**
		c)	Implement the following Boolean function (i) Y=f(a,b,c,d)= ∑m(0,1,2,4,6,9,12,14) using 4:1 MUX with 'a' and 'b' as select lines. (ii) Z=f(a,b,c,d)= ∑m(0,1,3,4,7,10,11,14,15) using 8:1 MUX with 'a' as input line	***CO 1***	***PO 1***	**8**
			OR			
	4	a)	Implement the following functions on 3x4x2 PLA. $F_1(X,Y,Z) = \sum m(0,1,3,4)$ $F_2(X,Y,Z) = \sum m(1,2,3,4,5)$	***CO 1***	***PO 1***	**8**
		b)	Design a priority encoder for a system with 3 inputs, the middle bit with highest priority encoding to 10, the MSB with the next priority encoding to 11, while the LSB with least Priority encoding to 01.	***CO 3***	***PO 3***	**8**
		c)	Design a 1-bit comparator using 2:4 decoder giving three outputs Greater(G), Equal(E), and Lower(L).	***CO 3***	***PO 3***	**4**
			UNIT - III			
	5	a)	Obtain the characteristic equation for SR and JK flip flops.	***CO 1***	***PO 1***	**5**
		b)	Using a positive edge triggering SR flip flop, design a counter which counts in the following sequence: 000,111,110,101,100,011,010,001,000…	***CO 3***	***PO 3***	**10**
		c)	Design a 4-bit universal shift register using D flipflops and MUX with mode selection inputs S1 and S0. The register operates as follows: S1 | S0 | Register Operation 0 | 0 | No change 0 | 1 | Complement 1 | 0 | Clear to 0 1 | 1 | Load parallel data	***CO 3***	***PO 3***	**5**
			OR			
	6	a)	Design a MOD-6 asynchronous ripple counter using T Flip flops.	***CO 3***	***PO 3***	**8**
		b)	Design JK flip flop from SR flip flop.	***CO 3***	***PO 3***	**6**
		c)	Explain how switch debouncing can be rectified with circuit and timing diagram.	***CO 1***	***PO 1***	**6**
			UNIT - IV			
	7	a)	Design the sequential circuit for the state diagram given below using JK-Flipflops	***CO 3***	***PO3***	**10**

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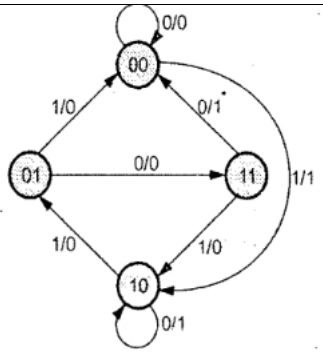
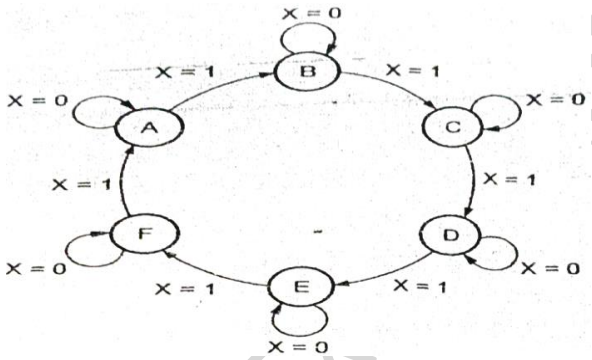
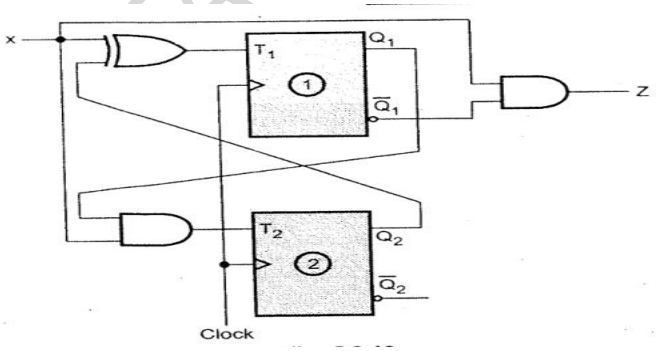
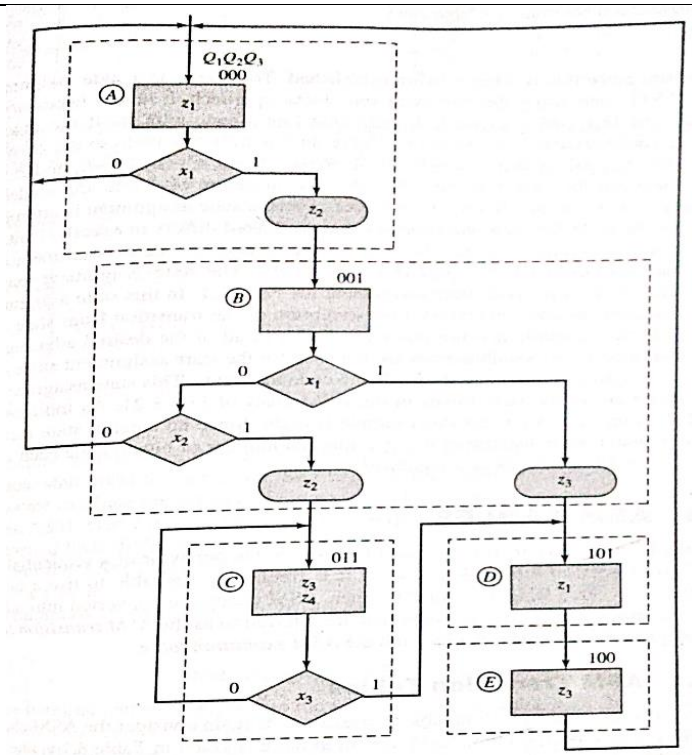
						
		b)	Design a Moore type sequence detector (using D-flip flop) to detect sequence "1101".	***CO 3***	***PO 3***	**10**
			OR			
	8	a)	Design a sequential circuit using D-FF for the given state diagram. Assume state assignment as A=000, B=010, C=011, D=101, E=110, and F=111 	***CO 3***	***PO 3***	**10**
		b)	Analyze the circuit shown and obtain the, state table and state diagram. 	***CO 2***	***PO 2***	**10**
			UNIT - V			
	9	a)	Develop the ASM chart for the following state machine: A two bit up counter with output Q_1Q_0 and enable signal 'X' is to be designed. IF 'X=0, counter changes the state as 00-01-10-11-00. If X=1, counter should remain in present state. Design a circuit using JK-flipflop.	***CO 3***	***PO 3***	**10**
		b)	Design a circuit for the following ASM chart using D-flipflop.	***CO 3***	***PO 3***	**10**

						
			OR			
	10	a)	Draw state diagram for Mealy state machine to detect sequence "1010" and also construct ASM chart for the same.	***CO 3***	***PO 3***	**10**
		b)	Design a ASM chart for 2 bits counter, if input line C=1 it works as up-counter otherwise it works as a down-counter. If it reaches to maximum value output turns to be high otherwise low.	***CO 3***	***PO 3***	**5**
		c)	Design an ASM chart to recognize the sequence X_1X_2=01,01,11,00.	***CO 3***	***PO3***	**5**

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