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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC3PCDSD **Max Marks: 100**
Course: Digital System Design **Date: 08.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) Simplify the given function using K-Map. Implement the simplified logic function using basic gates. **07**

$$F(W,X,Y,Z) = \sum m(3,5,6,7,8,9,10) + dc(4,11,12,14,15)$$

b) Explain the Verilog data types with syntax and example. **07**

c) Explain the port connections rules followed in Verilog HDL programming. **06**

UNIT - II

2 a) Derive logic expressions for 2-bit magnitude comparator and implement the same using Verilog data flow description. **12**

b) Design a 16x1 Multiplexer using 4x1 multiplexer. Write the truth table of 4x1 and 16x1 multiplexer. **08**

UNIT - III

3 a) Design an N-bit Asynchronous counter with JK flip-flop using Verilog generate statement. **10**

b) Explain the Verilog HDL case statements. Apply the concept of case statement, write the Verilog code to implement the encoder represented by the following truth table. Also write the test bench to test the functioning of the encoder given. **10**

Input(a)	Output(b)
xxx1	1
xx10	2
x100	4
1000	8
Others	0

OR

4 a) Below is a block with nested sequential and parallel blocks. Analyze, when does the block finish, what is the order of execution of events and at what simulation time does each statement finish execution? **10**

```
always
begin
     #4 Dry = 5;
     fork
       #6 Cun = 7;
       begin
          Exe = Box;
          #5 Jap = Exe;

       #2 Dop = 3;
       #4 Gos = 2;
       #8 Pas = 4;
     join
     #8 Bax = 1;
    #2 Zoom = 52;
    #6 $stop ;
end
```

b) Explain Verilog loop statements with syntax and example. Generate the clock pulse of time period 40ns with 10% duty cycle using forever statement. Initially clock is at logic 1 at 0ns. **10**

UNIT - IV

5 a) Design synchronous counter for sequence: $0 \rightarrow 1 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 7 \rightarrow 0$ using T flip-flop. Assume the unused sequences don't care. **10**

b) Derive the characteristic equation of JK flip-flop. **05**

c) Implement SR flip-flop using Verilog behavioral description. **05**

OR

6 a) Design a 4-bit universal shift register using a multiplexer and flip-flop to perform the operation as given in the below table. Explain the design with a relevant flip-flop and multiplexer truth table. **10**

S0	S1	Mode of Operation
0	0	No-Change
0	1	Shift-left
1	0	Shift-Right
1	1	Parallel-load

b) Convert D flip-flop to T flip-flop. **05**

c) Implement a counter to count the sequence 0-3-7-2-0 using Verilog HDL behavioral description. **05**

UNIT - V

7 a) Analyze the synchronous sequential circuit given in fig 1, write the transition table and state diagram. **10**

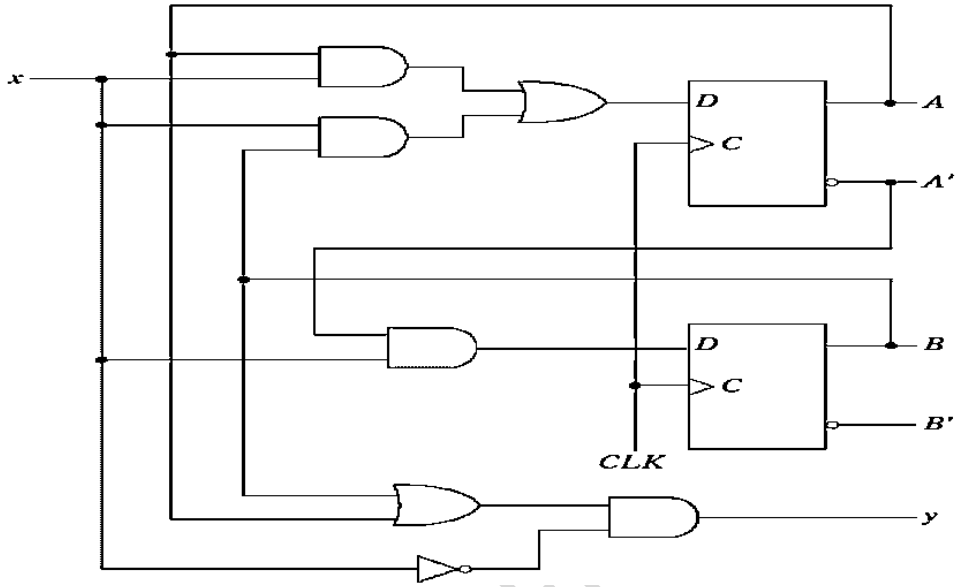

fig 1

b) Design a Moore sequence detector to detect the sequence 11011 using Verilog behavioral description by considering non-overlapping condition for the sequence. **10**

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