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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

December 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC3PCDSD **Max Marks: 100**
Course: Digital System Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Design a 2 bit, 2X1 Multiplexer with two inputs, A and B, each is of 2 bits wide and one select line, using only 2 input NAND Gates and describe it in Verilog Dataflow using ternary operator. **08**

b) Simplify the Boolean Function Y = F (A, B, C, D) = ∑m (0,6,8,13,14) +d (2,4,10), using K-Maps for both SOP and POS forms. **08**

c) Given A = 8'b10011100; **04**
   i. assign Y as Arithmetic right shift on A using any of the available operators in Verilog.
   ii. Evaluate ^A
   iii. Evaluate A | ~A
   iv. Evaluate A && ~A

UNIT - II

2 a) Design an eight-bit magnitude comparator using 1 to 4 Demultiplexer, and describe its behavior structurally in Verilog. **10**

b) Design a BCD adder using parallel adders. Draw its logic circuit and describe its behavior structurally in Verilog. **10**

UNIT - III

3 a) Design and Describe the behavior of a SORTING logic, that finds the maximum (MAX) and minimum (MIN) of five inputs, A, B, C, D and E. (Each input is 3 bits). Draw its block diagram and then describe it behaviorally in Verilog. **10**

b) Design a circuit that multiplies 5 to a BCD input and generates a BCD output, behaviorally Describe this design in Verilog HDL. **10**

OR

4 a) Design a Priority Encoder according to the Table Below and Describe its behaviour using behavioural descripting in Verilog HDL. **10**

Inputs					Outputs
Reset(R)	Enable(E)	A	B	C	Y
1	X	X	X	X	0
0	0	X	X	X	Y
0	1	1	X	X	2'd1
0	1	0	1	X	2'd2
0	1	0	0	1	2'd3
0	1	0	0	0	Y

b) Provide the Verilog code for the following specifications based on conditional instantiation **10**
1-Bit-adder for the first case
2-Bit-adder for the second case
4-Bit-parallel adder for the default case.

UNIT - IV

5 a) Design a D-Flip-flop from a D-latch, and write its behavior in Verilog HDL. **10**

b) Explain Ring counter and Johnson counter with truth table and circuit diagram. **10**

OR

6 a) Design a self-correcting synchronous counter, that counts the following sequence 3-5-6-7-2-1-3 ……repeats, using SR Flip-flop. **10**

b) "Race-around condition" How is this term associated with Flip-flops and latches explain? **04**

c) Using Shift Registers, design a frequency divider logic circuit to divide the frequency by 4. **06**

UNIT - V

7 a) Design a state machine for the sequence 110. Also write Verilog HDL code for the same. **10**

b) Analyze the below given synchronous sequential circuit, write the transition table and state diagram for the circuit shown in fig 1. **10**

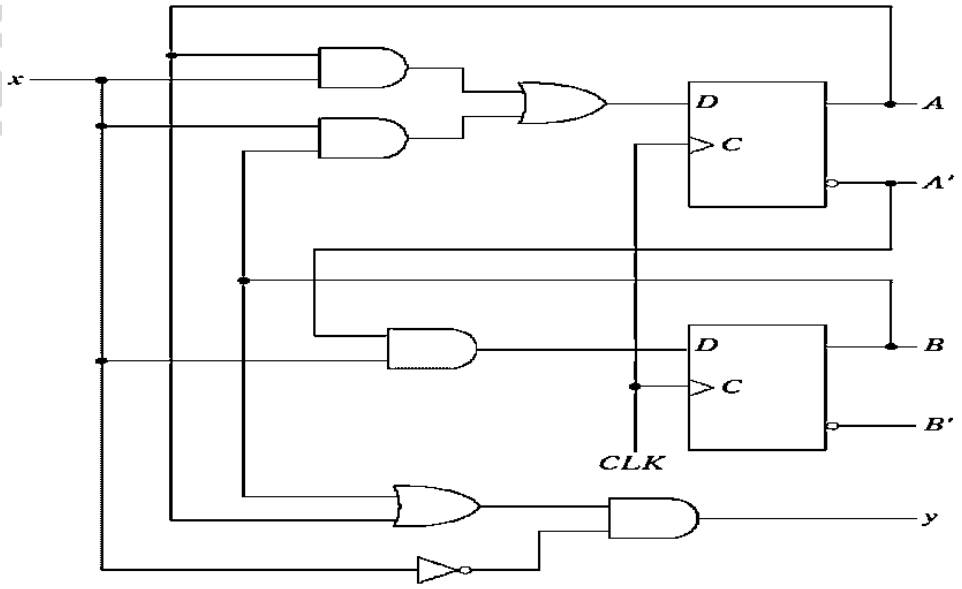

fig 1

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