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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC3PCDSD **Max Marks: 100**
Course: Digital System Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Simplify the following expression using K-map and draw the logic diagram for the same F(A, B,C,D) = ∏M (3,6,7,9,11,12,13,14,15) + d(0,2)	*CO 1*	*PO 1*	**10**
	b)		With an example for each, explain the relational, reduction, concatenation, and replication operators used in Verilog.	-	-	**10**
			UNIT - II			
2	a)		Design a 3:8 decoder Verilog module instantiating 2:4 decoders. The 2:4 decoder is to be implemented using gate-level modelling. Also write the test-bench to verify the functionality of the 3:8 decoder thus designed.	*CO 3*	*PO 3*	**10**
	b)		Implement the following function f1(x,y,z) = Σm (1,2,3,7) and f2 (x,y,z)= Σm(0,1,2,6) using 3x4x2 PLA. Write the PLA table.	*CO 1*	*PO 1*	**10**
			UNIT - III			
3	a)		Use "forever" construct to generate a clock with time-period=40ns and a duty cycle of 15%, with initial value '0'.	*CO 1*	*PO 1*	**5**
	b)		Write a Verilog program to calculate factorial of a 6-bit positive integer.	*CO 1*	*PO 1*	**7**
	c)		Design a 4-bit priority encoder with LSB having the highest priority. Describe its behavior using behavioral descripting in Verilog HDL. Write the testbench to test the designed encoder.	*CO 3*	*PO 3*	**8**
			OR			
4	a)		Apply the concept of blocking and non-blocking statements to develop two Verilog modules, respectively, to swap the contents of two registers: • with a temporary register • without a temporary register	*CO 1*	*PO 1*	**5**
	b)		Design a 4-bit ripple-carry adder using "generate" blocks. Instantiating full-adder modules implemented using half-adders.	*CO 3*	*PO 3*	**7**
	c)		Evaluate the below Verilog code. Analyse and write the time instances and the values of each of the variable used here. Justify the same.	*CO 2*	*PO 2*	**8**

```
module test();
   reg x,y,r,s,p,m;
      initial
         begin
           x = 1'b0;
           #5 y = 1'b1;
           fork
               #20 r = x;
               #15 s = y;
           join
           #40 x = 1'b1;
           fork
               #10 p = x;
               begin
                 #10 r = y;
                 #20 s = x;
               end
               #5 m = y;
           join
         end
endmodule
```

UNIT - IV

5 a) Describe the behavior of the **SHIFT REGISTER** given below using Verilog. Draw the schematic for reference.

Mode Control		Register Operation
S1	S0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel load

CO 3 *PO 3* **10**

b) Design a synchronous counter for the counting sequence of **0-2-4-6-7-0** using T flip-flops. Assume that all the unused states make transition to count value '0'. *CO 3* *PO 3* **10**

OR

6 a) Describe the behavior of T flip-flop in Verilog. Instantiate the same to implement a 3-bit asynchronous up-counter. Also write a test-bench to test the same. *CO 3* *PO 3* **10**

b) Implement the following:
(i) JK flip-flop using D flip-flop
(ii) JK flip-flop using SR flip-flop
CO 1 *PO 1* **10**

UNIT - V

7 a) Design a Mealy Serial Adder using necessary combinational logic and D flip-flops. *CO 3* *PO 3* **10**

b) Design a sequence detector using Verilog to detect overlapped "0101" sequence. Also write the test bench to test the design. *CO3* *PO 3* **10**

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