U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC3PCDSD **Max Marks: 100**
Course: Digital System Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Write the dataflow Verilog HDL code for a single bit magnitude comparator.	CO1	PO 1	6
	b)	List and describe different Verilog operators	CO 1	PO 1	4
	C)	Simplify the following expression using K-map and draw the logic diagram for the same F(A,B,C,D) = ∑ m (0,2,3.6,7) + d(8,10,11,15)	CO 1	PO 1	10
		UNIT - II			
2	a)	Design a 8X1 multiplexer using 4X1 multiplexers.	CO 3	PO 3	5
	b)	Implement full adder using multiplexer.	CO 1	PO 1	5
	c)	Design a comparator to compare the two 2 bit numbers using K-Map minimization.	CO 3	PO 3	10
		UNIT - III			
3	a)	Generate a clock with time period = 40 units and a duty cycle of 50%, using forever loop statement.	CO 1	PO 1	4
	b)	Design an n-bit adder using the parameter feature and Verilog generate statement.	CO 3	PO 3	10
	c)	Differentiate the blocking and Non-blocking statements using a sample code and explain the functionality of the code	CO 1	PO 1	6
		OR			
4	a)	Design a 4X2 Priority Encoder which functions when reset=0 and enable =1 to set the priority during encoding Describe its behavior using behavioral descripting in Verilog HDL	CO 3	PO 3	10
	b)	Design 4-bit ripple carry adder using for-loop and behavioral modeling.	CO 3	PO 3	10

			UNIT - IV			
	5	a)	Build the positive edge triggered master slave flip flop using D latches /Flip-flops. Explain its working principle.	***CO 1***	***PO 1***	**10**
		b)	Implement the JK flip-flop using Verilog behavioral modeling. Write the test code to test the functionality.	***CO 1***	***PO 1***	**10**
			OR			
	6	a)	Design a universal shift register with the help of 4X1 Mux to perform different operation of Hold, shift right, shift left and parallel load. Explain its functionality in detail.	***CO 3***	***PO 3***	**10**
		b)	Realize the JK flip-flop using SR flip-flop. Write the truth table and NAND structure for both the flip flops.	***CO 1***	***PO 1***	**10**
			UNIT - V			
	7	a)	Differentiate the Mealy and Moore FSM with examples state diagrams	***CO 1***	***PO 1***	**10**
		b)	Design the mealy FSM using Verilog HDL coding to detect the sequence 1001 by considering the overlapping case.	***CO 3***	***PO3***	**10**

****