U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

August 2023 Semester End Make-Up Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC3PCDSD **Max Marks: 100**
Course: Digital System Design **Date: 16.08.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1	a)	Simplify the following function using K-map method and also construct logic circuit for the simplified equation(function). $Y = f(a,b,c,d) = \sum(0,1,2,4,5,6,8,9,10,12,13,14)$	**08**
	b)	Design a combinational logic circuit for valid single digit BCD data, the output is '1' whenever a number greater than 5 appears at the input.	**05**
	c)	Discuss the various data types used in Verilog HDL.	**07**

UNIT - II

2	a)	With the help of truth tables, design Binary to Gray code conversion and BCD to Ex-3 conversion.	**10**
	b)	Draw and explain the circuit for 3 to 8 decoder.	**04**
	c)	Write short notes on ROM and PLAs.	**06**

UNIT - III

3	a)	Differentiate between blocking & non-blocking assignment statements with relevant examples.	**06**
	b)	With a suitable example, explain 4-to-1 Multiplexer using Verilog HDL case statement.	**07**
	c)	Explain the Verilog HDL Generate case construct with a suitable example.	**07**

OR

4	a)	Mention the three methods of timing control and explain any two with examples.	**10**
	b)	Illustrate with examples Repeat loop and Forever loop.	**10**

B.M.S.C.E. - ODD SEM 2022-23