U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

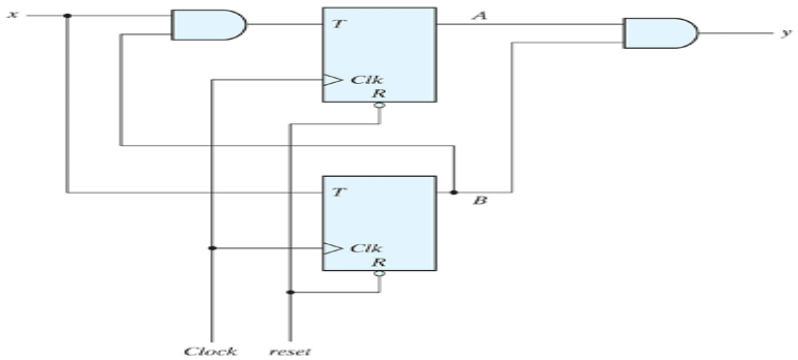
June 2025 Semester End Main Examinations

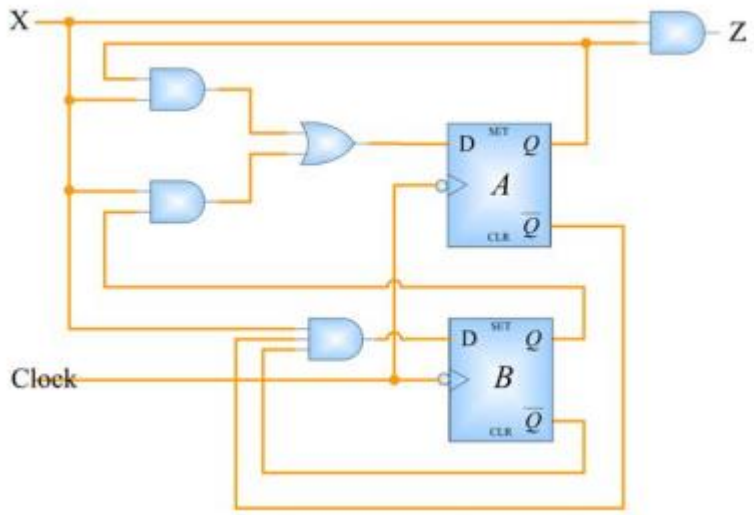
Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC3PCDSD **Max Marks: 100**
Course: Digital System Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

				CO	*PO*	Marks
			UNIT – I			
1	a)		Reduce the expression $f(P,Q,R,S)=\sum m(0,2,5,7,9,11) + d(3,8,10,12,14)$ using K-MAP and implement using NAND logic.	*CO* 1	*PO1*	**10**
	b)		Explain the operators used in Verilog HDL with syntax and examples.	-	-	**10**
			OR			
2	a)		Explain the VLSI design flow with neat flow diagram.	-	-	**10**
	b)		$f(P,Q,R,S) = \pi M(0,2,5,4,9,11) + d(1,8,10,14)$ using K-MAP and implement using NOR logic.	*CO* 1	*PO1*	**10**
			UNIT – II			
3	a)		Design a 4-bit Ripple Cary adder using Verilog HDL by instantiating Full adders.	*CO* 3	*PO3*	**10**
	b)		Design a 2-bit comparator with a relevant truth table, k-map, logical expressions, and logic diagram.	*CO* 3	*PO3*	**10**
			OR			
4	a)		Design a 4-bit BCD adder using parallel adders and with neat logic diagram, truth table and logic expression.	*CO* 3	*PO3*	**10**
	b)		Design a 2-bit assigned array multiplier using Verilog gate level description with neat logic diagram and logical expressions.	*CO* 3	*PO3*	**10**
			UNIT - III			
5	a)		Explain the Verilog conditional and multiway branching statement with examples.	-	-	**10**
	b)		Design a 16x1 Multiplexer by instantiating 4x1 multiplexers using Verilog HDL. Also write the behavioral description for 4x1 multiplexers. Also write the test bench to test the functionality.	*CO* 3	*PO3*	**10**
			OR			
6	a)		Explain the Verilog timing control statements with examples for each.	-	-	**10**

		b)	Design an 8-to-3 priority encoder using a Verilog case statement with the help of the truth table of the encoder. Also write the test bench to test the logic.	***CO*** 3	***PO3***	**10**
			UNIT - IV			
	7	a)	Derive the characteristic equation for the JK and SR flip-flops.	*CO1*	*PO1*	**6**
		b)	Design a 3-bit synchronous counter using D-flip-flip.	*CO3*	*PO3*	**10**
		c)	Design a JK Flip-flop by applying Verilog if-else-if statement.	*CO3*	*PO3*	**4**
			OR			
	8	a)	Convert D Flip-flop to SR flip flop and T-flip-flop to D flip-flop.	*CO1*	*PO1*	**6**
		b)	Design a 4-bit universal shift register to perform following Operations given in table below. Explain the design in detail. **S0** **S1** **Mode of Operation** 0 0 Locked state (No change) 0 1 Shift-Left 1 0 Shift-Right 1 1 Parallel Loading	*CO3*	*PO3*	**10**
		c)	Design shift-left and shift-right registers using Verilog case statement.	*CO3*	*PO3*	**4**
			UNIT – V			
	9	a)	Analyse the below given circuit and obtain the state diagram. 	CO2	***PO2***	**10**
		b)	Design a Verilog Moore FSM with one input X and one output Z. The FSM asserts its output Z when it recognizes the following input sequence:"1011". Also write the test code to test the functionality of the design.	***CO3***	***PO3***	**10**
			OR			

	10	a)	Design a Verilog Mealy FSM with to detect the sequence “101”. Also write the test code to test the functionality of the design.	***CO3***	***PO3***	**10**
		b)	Analyse the below given circuit and obtain the state diagram. 	CO2	***PO2***	**10**

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