U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June / July 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 23EC3ESHDL **Max Marks: 100**
Course: HDL Programming

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Explain the design flow of VLSI IC circuits.	-	-	**10**
	b)		Explain the components of a Verilog module with neat diagram.	-	-	**10**
			UNIT - II			
2	a)		Design a 4 to 1 multiplexer with block diagram, truth table, logic diagram and Verilog gate level description.	***CO 3***	***PO 3***	**10**
	b)		Analyse the Verilog operators used to perform shift operations with example.	***CO 2***	***PO 2***	**10**
			UNIT - III			
3	a)		Distinguish between blocking and non-blocking assignments with examples.	***CO 1***	***PO 1***	**10**
	b)		Analyse the methods of timing control used in Verilog with an example.	***CO 2***	***PO 2***	**10**
			OR			
4	a)		Write a program to display count value from 0 to 127 also write the test code.	***CO 1***	***PO 1***	**10**
	b)		Design n-bit comparator using verilog behavioral modeling which can be reused in different designs. The code should define the value of output at its every case of comparison also write testbench for the same.	***CO 3***	***PO 3***	**10**
			UNIT - IV			

5	a)		Analyse the given code segment and
			i) Complete the code as per your understanding.
			ii) Draw the logic diagram expected after synthesis.
			module ……
			…….
			assign sel[0] = en1?1'b0:1'b1;
			assign sel[1]=en2? 1'b0:1'b1;
				CO 2	***PO 2***	**10**

			case (sel) 2'b00: out = a; 2'b01: out = b; 2'b10: out = c; 2'b11: out = d; endcase assign y=out & endmodule			
		b)	Draw and explain the logic synthesis flow from RTL to Gates.	-	-	**10**
			UNIT - V			
	6	a)	With a neat block diagram and example, explain the Mealy and Moore model in a sequential circuit analysis.	-	-	**10**
		b)	Design a Mealy type sequence detector to detect the sequence of 101 in the given sequence of 001101100101011 using Verilog for the overlapping condition.	***CO 3***	***PO 3***	**10**
			OR			
	7	a)	Design a mealy type serial adder using Verilog HDL.	***CO 3***	***PO 3***	**10**
		b)	Design a mealy sequential circuit using Verilog to convert BCD to Excess 3 code with state diagram.	***CO 3***	***PO3***	**10**

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