U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 23EC3ESHDL **Max Marks: 100**
Course: HDL Programming

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			UNIT - I	CO	PO	Marks
1	a)		Discuss the top down design Methodologies with an example of 4 to 16 decoder using 2 to 4 decoders.	CO 1	PO 1	10
	b)		Discuss in detail the typical VLSI design flow with diagram.	-	-	10
			UNIT - II			
2	a)		Develop a data flow description to implement the logic mentioned below: B is a BCD input, while Y is a BCD output, the logic multiplies B with 5 and generates Y.	CO 3	PO 3	8
	b)		Design a Carry look ahead adder , assuming FULL ADDER delay to generate SUM as 2 ns and Carry as 4 ns	CO 3	PO 3	12
			UNIT - III			
3	a)		Analyze the usage of Verilog "if-else-if" block for describing the behavior of an 4-Bit comparator also write the test code.	CO 2	PO 2	10
	b)		Design a clock generator that divides the input clock by 3 with a duty cycle of 50%.	CO 3	PO 3	10
			OR			
4	a)		Design a JK flip-flop with a case statement on output Q also write the testbench to test the functionality.	CO 3	PO 3	8
	b)		Design a 4 bit loadable-synchronous counter as described in the below table. Also write the test bench.	CO 3	PO 3	12

CLK	Reset	Load	output Q[3:0]
Rising Edge	1	X	4'd0
	0	1	Load_value
	0	0	Q+1

			UNIT - IV			

	5	a)	Analyse the given code, write the Synthesized logic diagram
			
			`module A(W,X,Y,Z);`
			`input W,X,Y;`
			`output Z;`
			`reg R;`
			
			`assign Z = R;`
			
			`always@(negedge W or posedge X)`
			`begin`
			`if(X) R <= 0;`
			`else if(Y) R <= ~R;`
			`end`
				CO 2	***PO 2***	**8**

		b)	Analyse the given code segment and
			i) Complete the code as per your understanding.
			ii) Draw the logic diagram expected after synthesis.
			
			module ……
			…….
			assign sel[0] = en1?1'b0:1'b1;
			assign sel[1]=en2? 1'b0:1'b1;
			case (sel)
			2'b00: out = a;
			2'b01: out = b;
			2'b10: out = c;
			2'b11: out = d;
			endcase
			assign y=out &
			endmodule
				CO 2	***PO 2***	**12**

			UNIT - V			
	6	a)	Explain the general architecture of FPGA	-	-	**8**
		b)	Design a BCD to Excess-3 Mealy FSM using Verilog HDL. For this design draw the state diagram. Write the required test bench to verify its functionality.	***CO 3***	***PO 3***	**12**
			OR			
	7	a)	Design a Mealy FSM to detect the non-overlapping sequence 1010 using Verilog HDL	***CO 3***	***PO 3***	**10**
		b)	Identify the type of FSM from the below State Table 1.1 And complete the output Z values from Table 1.2 also write the Verilog code to implement the given FSM.	***CO 2***	***PO2***	**10**

Present State(PS)	INPUT (X)	Next State(NS)	Output(Z)
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

Table 1.1

Time(ns)	X	Z
0	0	
5	1	
10	0	
20	1	
25	0	
30	1	
35	1	
40	1	
45	0	
50	0	
60	0	
65	1	
70	1	
80	0	
85	1	
90	1	
100	0	

Table 1.2

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