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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 23EC3ESHDL **Max Marks: 100**

Course: HDL Programming

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

				CO	PO	Marks
			UNIT - I			
1	a)		With a neat diagram, explain the design flow of VLSI IC circuits.	--	--	**10**
	b)		Design a 4-bit ripple carry counter in the bottom-up design methodology, assuming only D flip-flop and NOT gate as building blocks.	CO3	PO3	**10**
			OR			
2	a)		Design a 4-bit parallel adder using top-down design methodology assuming appropriate leaf cells.	CO3	PO3	**10**
	b)		Explain the Verilog data types with an example.	--	--	**10**
			UNIT - II			
3	a)		Design a 8-to-1 multiplexer using only 2-to-1 multiplexers as building blocks. Also realize the 2-to-1 multiplexer using dataflow modeling.	CO3	PO3	**10**
	b)		What are the different types of gate delays in logic circuits, and how can they be modeled using a Verilog module?	--	--	**10**
			OR			
4	a)		Explain continuous assignment statements used in dataflow modeling using examples of arithmetic and logical operators.	--	--	**10**
	b)		Design a 3-bit carry lookahead adder using dataflow modeling. Also write the stimulus block to test the Verilog module thus developed.	CO3	PO3	**10**

			UNIT - III			
	5	a)	Design a 4-bit modulo-10 reset-able synchronous up/down counter which counts up if input X is high and counts down otherwise using behavioural modeling.	***CO3***	***PO3***	**10**
		b)	How can delay-based timing control be applied in Verilog? Explain both methods of timing control with a suitable example.	--	--	**10**
			OR			
	6	a)	Write a Verilog loop statements along with an example of each.	--	--	**10**
		b)	Design a 4-bit universal shift register with modes of parallel load, left shift with serial input, right shift with serial input, circular left shift, circular right shift and hold.	***CO3***	***PO3***	**10**
			UNIT - IV			
	7	a)	Explain the concept of logic synthesis and its importance in digital design. Discuss how the process has evolved from manual schematic design to modern automated tools, highlighting the role of the standard cell library and design constraints.	--	--	**10**

		b)	Analyze the Verilog code snippet given below. Complete the module description and write the synthesized logic circuit.
			`always @(inp)`
			`begin`
			`  if (inp[0] == 1'b1)`
			`  outp = 3'd7;`
			`  else if (inp[1] == 1'b1)`
			`  outp = 3'd6;`
			`  else if (inp[2] == 1'b1)`
			`  outp = 3'd5;`
			`  else`
			`  outp = 3'd0;`
			`end`
				CO2	***PO2***	**10**

			OR			
	8	a)	Draw and explain the logic synthesis flow from RTL to Gates.	--	--	**10**

		b)	Analyze the following code snippet and complete the Verilog module description. Also draw the logic diagram expected after synthesis.
			`module ____________`
			`____________________`
				CO2	***PO2***	**10**

			assign sel[0] = en1 ? 1'b0 : 1'b1;
			assign sel[1] = en2 ? 1'b0 : 1'b1;
			case (sel)
			2'b00: out = a;
			2'b01: out = b;
			2'b10: out = c;
			2'b11: out = d;
			endcase
			assign y = out;
			endmodule			

			UNIT - V			
	9	a)	Differentiate between Mealy and Moore machines with the help of a suitable example.	--	--	**10**
		b)	Design a Verilog module to convert BCD to Excess 3 code with the help of state diagram.	***CO3***	***PO3***	**10**
			OR			
	10	a)	Design a Mealy type sequence detector to detect the sequence of 101 with overlapping allowed on a single bit input stream.	***CO3***	***PO3***	**10**
		b)	With the help of neat diagrams, briefly describe the building blocks of SRAM-based FPGA.	--	--	**10**

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