U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code:23EC3ESHDL **Max Marks: 100**
Course: HDL Programming

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Discuss the rules to be followed while connecting the Verilog ports with an example code.	CO1	PO 1	5
	b)	Discuss the difference between Monitor and Display statements with example.	CO 1	PO 1	4
	c)	Design a 4-bit T flip-flop based Ripple- Carry counter using top-down design methodology. Also write the test bench to generate clock and reset inputs.	CO 3	PO 3	11
		UNIT - II			
2	a)	Design a 2x2 unsigned array multiplier using Verilog data flow description. Also write the test bench to test the functionality.	CO 3	PO 3	8

	b)	Analyze the given Verilog code, Initial value of A=1, B=0, C=0, and G=0. 'A' changes from 1 to 0 and 'B' changes from 0 to 1 at time T0. 'C' changes from 0 to 1 at T1 . 'G' changes from 0 to 1 at T2. Given T0 = 100ns : T1 =200ns : T2 = 300ns. Output 'Y' will have changes at T0+Δ1 ,T1+Δ2,T2+Δ3. Find Δ1, Δ2, Δ3 in terms of ns.
		`module TEST1(A,B,C,G,Y);`
		`input A,B,C,G;`
		`output Y;`
		`wire S1,S2,S3,S4,S5;`
		`assign #7 Y=S4 | S5;`
		`assign #7 S4= A&S2&S1;`
		`assign #7 S5= B&S3&S1;`
		`assign #7 S2=~C;`
		`assign #7 S3 = ~S2;`
		`assign #7 S1=~G;`
		`endmodule`
			CO 2	PO 2	8

	c)	Develop a Verilog gate level model for the 4X1 Multiplexer using its gate structure.	CO 1	PO 1	4

			UNIT - III			
	3	a)	Design a N-bit Magnitude Comparator using Full-adder, write a Verilog code for a N- bit Magnitude Comparator Using Generate statement. Draw all the required logic diagrams.	***CO 3***	***PO 3***	**10**
		b)	Explain the structure of various loop statements in HDL with syntax and example code.	-	-	**6**
		c)	Develop a Serial-In-Serial-Out shift register using always statement.	***CO 3***	***PO 3***	**4**
			OR			
	4	a)	Design an 8-bit counter by using a forever loop, named block, and disabling of named block. The counter starts counting at count = 4 and finishes at count = 68. The count is incremented at positive edge of clock. The clock has a time period of 10. The counter counts through the loop only once and then is disabled.	***CO 3***	***PO 3***	**10**
		b)	Explain the blocking and non-blocking statements used in Verilog with example.	-	-	**6**
		c)	Develop a JK Flip-flop by applying Verilog case statement on output q.	***CO 3***	***PO 3***	**4**
			UNIT - IV			

	5	a)	Analyze the following snippet of Verilog code, write the complete Verilog description and interpreted logic diagram with combination of multiplexers and gates.
			`always @(x)`
			`begin`
			`if (x[0]) y = 2'b00;`
			`else if (x[1]) y = 2'b01;`
			`else if (x[2]) y = 2'b10;`
			`else if (x[3]) y = 2'b11;`
			`else y = 2'bxx;`
			`end`
				CO 2	***PO 2***	**6**

		b)	With flow diagram, explain the RTL to gate level logic synthesis flow.	-	-	**6**
		c)	Analyse the below given Verilog snippet, write the synthesed logic diagram and complete code. Assume X is a 2-bit vector. always @ (X) begin Y = 2 * X + 3; end	***CO 2***	***PO 2***	**8**
			UNIT - V			
	6	a)	Design a Verilog Moore FSM with one input X and one output Z. The FSM asserts its output Z when it recognizes the following input sequence:"1011". The machine will keep checking for the proper bit sequence and does not reset to the initial state after it recognized the string. Also write the test code to test the functionality of the design.	***CO 3***	***PO 3***	**10**
		b)	Explain the FPGA Architecture with the help of block diagram	-	-	**10**
			OR			
	7	a)	Design a Moore-type serial adder using Verilog behavioral description.	***CO 3***	***PO3***	**10**
		b)	Explain the FPGA design flow with block diagram.	-	-	**10**

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