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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

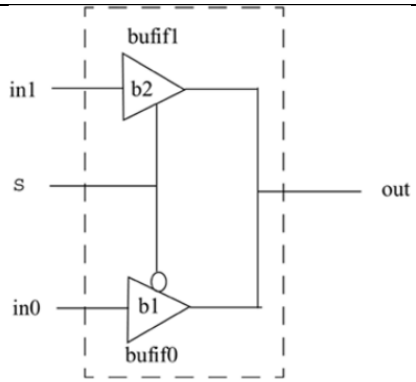
June 2025 Semester End Main Examinations

Programme: B.E. **Semester: IV**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC4PCHDL **Max Marks: 100**
Course: HDL Programming

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Explain the VLSI design flow with the help of a flow diagram.	-	-	**6**
	b)		Discuss the difference between monitor and display statements with example.	*CO 1*	*PO 1*	**4**
	c)		Design a 4-bit ripple-carry adder using Verilog top-down design methodology. Write the gate level implementation for the leaf cell.	*CO 3*	*PO 3*	**10**
			OR			
2	a)		Design a 4-bit ripple carry counter using Verilog top-down design methodology. Write the code foe each of the leaf cells.	*CO 3*	*PO 3*	**10**
	b)		Discuss the different types of descriptions used in Verilog with example code.	*CO 1*	*PO 1*	**10**
			UNIT - II			
3	a)		If A and B are two unsigned variable with A = 11110000 and B = 01011101, find the value of i. ~(A&B) ii. A && B iii. ~|B iv. B<<1	*CO 1*	*PO 1*	**8**
	b)		Design a logic system that has three 1-bit inputs, a_1,a_2 and a_3;and 1-bit output b. The LSB bit is a_1; and b is '1' only when $a_1a_2a_3$=1,3,6 and 7(all in decimal), otherwise b is 0. Write the Verilog data flow description to implement the design.	*CO 3*	*PO 3*	**8**
	c)		Design a Verilog gate level model for the 4X1 Multiplexer using its gate structure.	*CO 3*	*PO 3*	**4**
			OR			
4	a)		Design a 2-to-1 multiplexer using bufif0 and bufif1 gates as shown below. The delay specification for gates b1 and b2 are as follows:	*CO 3*	*PO 3*	**10**

			 **Min** **Typ** **Max** Rise 1 2 3 Fall 3 4 5 Turnoff 5 6 7 Write the Verilog code and apply stimulus to test the output values.			
	b)	If A, B and C are three unsigned variables with A = 1101 and B = 1010 and C = 0111. find the value of y = ((A ^ B) && (~^C))+((A>>>3)|(C<<2));	***CO 1***	***PO 1***	**10**
		UNIT - III			
5	a)	Design a N-bit magnitude comparator using full-adder, write a Verilog code for a N- bit magnitude comparator Using generate statement. Draw all the required logic diagrams.	***CO 3***	***PO 3***	**10**
	b)	Explain the syntax of Verilog if-else statement and case statement with example.	-	-	**6**
	c)	Differentiate task and functions.	***CO 1***	***PO 1***	**4**
		OR			
6	a)	Design an 8-bit counter by using a forever loop, named block, and disabling of named block. The counter starts counting at count = 4 and finishes at count = 68. The count is incremented at positive edge of clock. The clock has a time period of 10. The counter counts through the loop only once and then is disabled.	***CO 3***	***PO 3***	**10**
	b)	Explain the structure of various loop statements in HDL with syntax and example code.	-	-	**6**
	c)	Design a SR Flip-flop by using Verilog case statement.	***CO 3***	***PO 3***	**4**
		UNIT - IV			
7	a)	With flow diagram, explain the RTL to gate level logic synthesis flow.	-	-	**8**
	b)	Analyse the function given below and write the complete code and synthesized logic diagram. function [3:0] fact; input [2:0] a; begin if (a<=4) fact = 2*a+5; end endfunction	***CO 2***	***PO 2***	**12**
		OR			

	8	a)	List the synthesizable Verilog constructs, and explain how logic synthesis tools interpret the following Verilog constructs: (a) Assign (b) if-else (c) case	-	-	**10**

		b)	Analyze the below given code snippet. Write the complete Verilog code and Synthesized logic circuit.
			
			always @(inp)
			begin
			if (inp[0] == 1'b1)
			outp = 3'd7;
			else if (inp[1] == 1'b1)
			outp = 3'd6;
			else if (inp[2] == 1'b1)
			outp = 3'd5;
			else
			outp = 3'd0;
			end
				CO 2	***PO 2***	**10**

			UNIT - V			
	6	a)	Design a Mealy type FSM for Ex-3 to BCD code converter using Verilog with a relevant state diagram.	***CO 3***	***PO 3***	**12**
		b)	Explain the FPGA architecture with the help of a block diagram	-	-	**8**
			OR			
	7	a)	Design a Mealy-type FSM for serial adder using Verilog behavioral description with the relevant state diagram.	***CO 3***	***PO3***	**11**
		b)	Explain the following with respect to FPGA design: i. Design Implementation ii. Static timing analysis iii. Back-Annotation	-	-	**9**

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