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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC5PE1AD **Max Marks: 100**
Course: Advanced Digital Logic Design **Date: 03.03.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1	a)	Design and implement the synchronous Mod-9 counter and develop the RTL with neat indentation, comments and header. For the counter module designed, develop the Verilog test bench which tests all possible test scenarios along with expected timing diagram.	**10**
	b)	Discuss the front end in ASIC design flow?	**10**

OR

2	a)	Design and develop the Verilog source code for a 4-bit shift register. Use any modelling technique and verify the functionality using a test bench.	**12**
	b)	Discuss Verilog full case and parallel case with a suitable example for each.	**08**

UNIT - II

3	a)	Discuss some of the general RTL coding guide lines. List some of the Non-Synthesizable verilog constructs.	**12**
	b)	Discuss Verilog event queue in detail.	**08**

UNIT - III

4	a)	What is black hole time? Evaluate maximum frequency of operation for a sequential circuit.	**08**
	b)	With neat illustrations, explain the setup time and hold time and derive the equations for setup time and hold time inequalities. Perform setup and hold analysis for the sequential circuit shown in Figure 1.	**12**

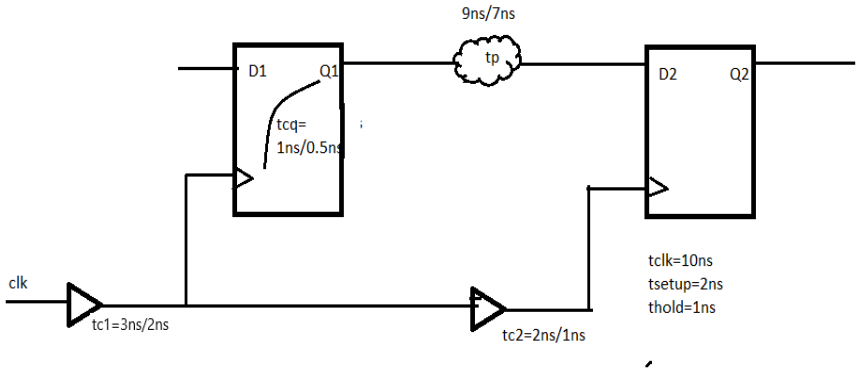

Figure 1

UNIT - IV

5	a)	Discuss the process of Translation, mapping and Optimization during logic synthesis.	**08**
	b)	What are standard cells? Discuss characterization goals and constraint driven optimization.	**12**

UNIT - V

6	a)	With neat illustrations, distinguish between Moore and Mealy state machines.	**05**
	b)	Draw the state diagram and develop the Verilog RTL for a Mealy state machine which produces output as '1' if the input bit stream is divisible by 5, with neat indentation, comments and header. Write the Verilog test bench for the same which tests the complete scenario of state transitions.	**15**

OR

7	a)	Draw the state diagram and develop the Verilog RTL for an overlapping Moore FSM which produces output '1' when the input bit stream is 1101 with neat indentation, comments and header. Write the Verilog test bench for the same which tests the complete scenario of state transitions.	**15**
	b)	Draw the state diagram of Mealy FSM to implement a T Flip Flop.	**05**

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