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B. M. S. College of Engineering, Bengaluru - 560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC5PE1AD **Max Marks: 100**
Course: Advanced Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

SUPPLEMENTARY EXAMS 2023

UNIT - I

1. a) Design and implement the asynchronous Mod-9 counter and develop the RTL with neat indentation, comments and header. For the counter module designed, develop the Verilog test bench which tests all possible test scenarios along with expected timing diagram. **10**

   b) Design and develop the Verilog source code for a 6:1 mux using 2:1 multiplexers. **10**

OR

2. a) Design and develop the Verilog source code for a 4-bit shift register. Use any modelling technique and verify the functionality using a test bench. **12**

   b) Discuss Verilog full case and parallel case with a suitable example for each. **08**

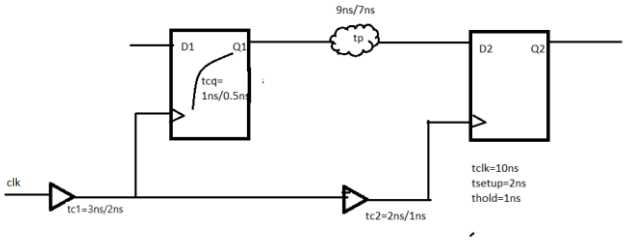
UNIT - II

3. a) Describe the guidelines that need to be followed while implementing Verilog RTL code. **10**

   b) Discuss the different types of delay models for behavioural modelling. **10**

UNIT - III

4. a) With neat labelled diagrams, explain the setup time and hold time and derive the equations for setup time and hold time inequalities. Perform setup and hold analysis for the sequential circuit shown. **12**



b) What is black hole time? Evaluate maximum frequency for a sequential circuit. **08**

UNIT - IV

5. a) What are standard cells? Discuss characterization goals and constraint driven optimization. **12**

b) Discuss the process of Translation, mapping and Optimization. **08**

UNIT - V

6. a) Develop the Verilog source code for an overlapped Mealy FSM which detects 101 sequence and produces output as y=1. Verify the functionality of the RTL by developing the test bench. **12**

b) Develop the Verilog source code for JK flip flop using D flip flop **08**

OR

7. Design and develop the Verilog source code for a non-overlapping Moore FSM which detects 001 or 100 sequences and produces output y=1. Verify the functionality of the RTL by developing the test bench. **20**

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SUPPLEMENTARY EXAMS 2023

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