U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

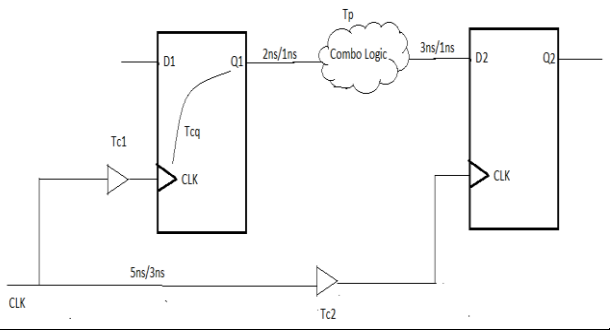
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

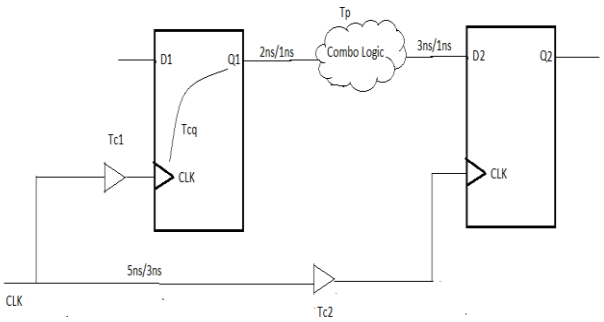
Course Code: 23EC5PE1AD / 22EC5PE1AD **Max Marks: 100**

Course: Advanced Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a		Design 4 bit ripple carry adder in structural description. Write test bench and timing waveforms.	***CO** 3*	*PO 3*	**10**
	b		Explain blocking and non-blocking statements with examples.	-	-	**10**
			OR			
2	a		Explain difference between task and function with examples.	-	-	**10**
	b		Design a 4 bit synchronous counter using Verilog. Write the test bench for the same.	***CO** 3*	*PO 3*	**10**
			UNIT - II			
3	a		Design a 8 to 1 multiplexer using case statement and write the test bench code in Verilog.	***CO** 3*	*PO 3*	**10**
	b		Discuss the different regions in the verilog event queue.	-	-	**10**
			OR			
4	a		Discuss the important Verilog coding guidelines.	-	-	**10**
	b		Design T-Flip Flop using D Flip Flop and write the test bench.	***CO** 3*	*PO 3*	**10**
			UNIT - III			
5	a		For the RTL shown, analyze timing to report violations. Given: T_{c1}= 2ns/1ns; T_c2= 2ns/1ns; T_p=8ns/7ns; T_{cq}=4ns/3ns; Tsetup=2ns; T_{hold}=1ns; T_{clk}=7ns. 	***CO** 2*	*PO 2*	**10**

		b	With the help of RTL, analyze the Setup and Hold inequalities.	***CO** 2*	*PO 2*	**10**
			OR			
	6	a	With the help of D flip flop, analyze the delays for T_{hold} and T_{setup}.	***CO** 2*	*PO 2*	**10**
		b	For the RTL shown, analyze timing to report violations. Given: T_{c1}= 3ns/2ns; T_c2= 3ns/2ns; T_p=9ns/8ns; T_{cq}=4ns/3ns; Tsetup=3ns; T_{hold}=2ns; T_{clk}=8ns. 	***CO** 2*	*PO 2*	**10**
			UNIT - IV			
	7	a	With neat illustrations, discuss various steps in logic systhesis.	-	-	**10**
		b	Discuss the main optimization trade-offs as applied to logic Synthesis.	***CO** 1*	*PO 1*	**10**
			OR			
	8	a	Discuss in detail the concept of Digital standard cell library.	-	-	**10**
		b	Discuss the importance of wire load models when applied to logic synthesis.	***CO** 1*	*PO 1*	**10**
			UNIT - V			
	9	a	Analyze some issues related to CDC designs.	***CO** 2*	*PO 2*	**10**
		b	Design a Non-Overlapping Moore Sequence Detector for the sequence 1101.	***CO** 3*	*PO 3*	**10**
			OR			
	10	a	Analyze data loss and its consequences in CDC designs.	***CO** 2*	*PO 2*	**10**
		b	Design Overlapping Mealy Sequence Detector to detect the sequence 1010.	***CO** 3*	*PO3*	**10**

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