U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2025 Semester End Make-Up Examinations

Programme: B.E. **Semester: V**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

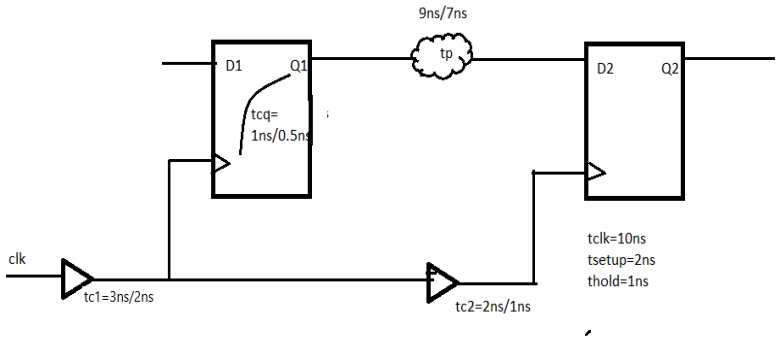
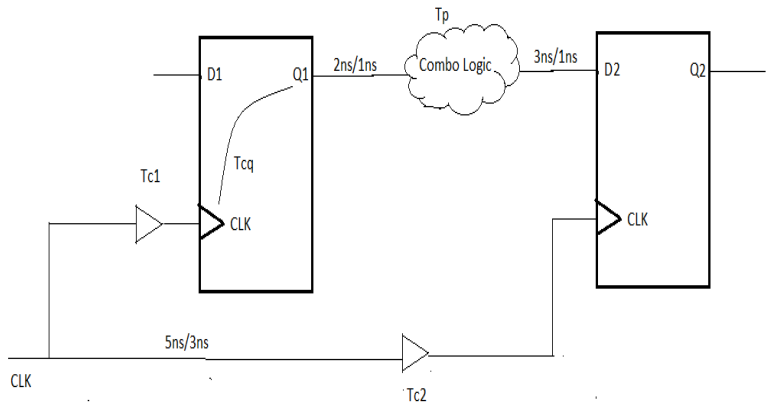
Course Code: 23EC5PE1AD / 22EC5PE1AD **Max Marks: 100**

Course: Advanced Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			CO	PO	Marks
		UNIT - I			
1	a)	Design and implement the asynchronous Mod-9 counter and develop the RTL with neat indentation, comments and header. For the counter module designed, develop the Verilog test bench which tests all possible test scenarios along with expected timing diagram.	*CO 3*	*PO 3*	**10**
	b)	Design and develop the Verilog source code for a 6:1 mux using 2:1 multiplexers.	*CO 3*	*PO 3*	**10**
		OR			
2	a)	Design and develop the Verilog source code for a 4-bit shift register. Use any modelling technique and verify the functionality using a test bench.	*CO 3*	*PO 3*	**12**
	b)	Develop an example code in Verilog to illustrate full case and parallel case constructs.	*CO 3*	*PO 3*	**08**
		UNIT - II			
3	a)	Describe the guidelines that need to be followed while implementing Verilog RTL code.	-	-	**10**
	b)	Analyse the different types of delay models for behavioural modelling.	*CO2*	*PO2*	**10**
		OR			
4	a)	Analyse how the active events, inactive events, NBA update events, Monitor events and future events gets executed in a Verilog event queue.	*CO2*	*PO2*	**10**
	b)	What are Non-synthesizable Verilog constructs. List them.	-	-	**10**

			UNIT - III			
	5	a)	With neat labelled diagrams, analyse with equations, the setup time and hold time inequalities for the sequential circuit shown. 	*CO2*	*PO2*	**12**
		b)	What is black hole time? Evaluate maximum frequency for a sequential circuit	*CO1*	*PO1*	**08**
			OR			
	6	a)	For the following figure, evaluate the setup time and hold time violations. Given: T_{c1}= 2ns/1ns; T_c2= 2ns/1ns; T_p=9ns/7ns; T_{cq}=4ns/3ns; Tsetup=2ns; T_{hold}=1ns; T_{clk}=6ns. 	*CO2*	*PO2*	**10**
		b)	Discuss timing concepts with respect to set-up and Hold. Derive the Set-up and Hold inequalities.	*CO1*	*PO1*	**10**

			UNIT - IV			
	7	a)	What are standard cells? Discuss characterization goals and constraint driven optimization.	-	-	**12**
		b)	Develop the Verilog source code for JK flip flop using D flip flop.	*CO3*	*PO* 3	**08**
			OR			
	8	a)	Develop the Verilog source code for an overlapped Mealy FSM which detects 101 sequence and produces output as y=1. Verify the functionality of the RTL by developing the test bench.	*CO3*	*PO* 3	**12**
		b)	Discuss the main optimization trade-offs. What are constraints and design goals?	-	-	**08**
			UNIT - V			
	9	a)	Design and develop the Verilog source code for a non-overlapping Moore FSM which detects 001 or 100 sequences and produces output y=1. Verify the functionality of the RTL by developing the test bench.	*CO3*	*PO* 3	**14**
		b)	What is Cross domain crossing? Analyze the issues related to CDC designs.	*CO2*	*PO2*	**06**
			OR			
	10	a)	Draw the state diagram and develop the Verilog RTL for a Mealy state machine which produces output as '1' if the input bit stream detects 1111 sequence with overlap. Write the Verilog test bench to test the same.	*CO3*	*PO* 3	**12**
		b)	Analyze the condition for data loss in CDC designs with neat timing diagrams.	*CO2*	*PO2*	**08**

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