U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

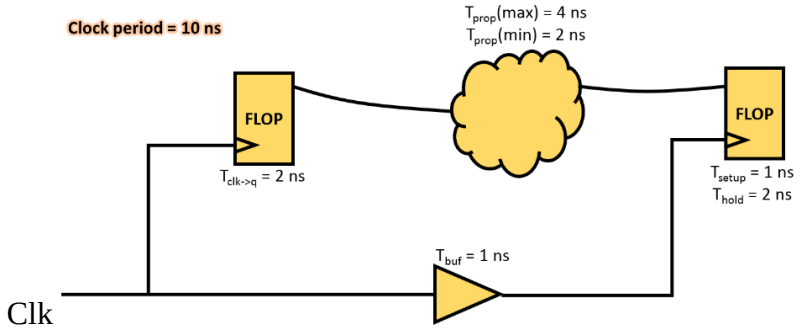
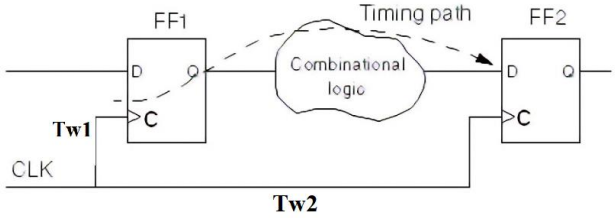
Course Code: 23EC5PE1AD / 22EC5PE1AD **Max Marks: 100**

Course: Advanced Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	***CO***	***PO***	**Marks**
1	a)		Discuss ASIC Design Flow in detail with neat flow diagram.	-	-	**08**
	b)		Design JK_FF using D_FF and Multiplexer. Write a test bench to test the same.	***CO** 3*	*PO3*	**12**
			OR			
2	a)		Write the Verilog RTL for a clock divided by 4 counter with 50% duty cycle and asynchronous active high reset condition. The design should have an output Y that goes high each time the count becomes 2. Also write a test bench for the same.	***CO** 3*	*PO3*	**12**
	b)		Discuss "always" and "initial" constructs in verilog with a suitable example for each.	-	-	**08**
			UNIT - II			
3	a)		Discuss non-synthesizable Verilog constructs and list any five.	-	-	**08**
	b)		Analyse the significance of Reset recovery time for asynchronous reset designs. Suggest a suitable method to ensure that the reset recovery time is met when using asynchronous reset.	*CO2*	*PO2*	**12**
			OR			
4	a)		Discuss Verilog event Queue with neat flow diagram.	-	-	**12**
	b)		Analyse with examples the various delay models for Data flow modelling.	*CO2*	*PO2*	**08**
			UNIT - III			
5	a)		With the example of negative edge triggered D Flip Flop, analyse the setup and hold time delays.	*CO2*	*PO2*	**10**
	b)		Analyze the RTL given below for set-up and hold violations.	*CO2*	*PO2*	**10**

						
			OR			
	6	a)	Analyse the approaches to fix the following violations: i) Setup violations ii) Hold violations	*CO2*	*PO2*	**10**
		b)	Analyse the RTL shown below for set-up and hold violations Given : T_{clk-q}= 4ns/1ns, T_p=7ns/5ns, T_{w1}=T_{w2}=2ns/1ns, T_{su}=5ns, T_h=1ns, T_{clk}=10ns. 	*CO2*	*PO2*	**10**
			UNIT - IV			
	7	a)	Applying the concept of logic Synthesis, discuss with neat diagrams the process of Translation, Mapping and optimization.	*CO1*	*CO 1*	**12**
		b)	Discuss the concept of DSCL and its content selection.	-	-	**08**
			OR			
	8	a)	Discuss the main optimization trade-offs.	-	-	**10**
		b)	In VLSI designs, apply the concept of constraints driving the optimization.	*CO1*	*CO 1*	**10**
			UNIT - V			
	9	a)	Draw the state diagram and develop the Verilog RTL for a Non-overlapping Moore FSM which produces output ‘1’ when the input bit stream is 1001 with neat indentation, comments and header.	***CO** 3*	*PO3*	**12**
		b)	Discuss and analyse data loss issue in CDC designs.	*CO2*	*PO2*	**08**
			OR			
	10	a)	Draw the state diagram and develop the Verilog RTL for a non-overlapping Mealy state machine which produces output as ‘1’ if the input bit stream is 1011 with neat indentation, comments and header.	***CO** 3*	*PO3*	**12**
		b)	Discuss and analyse Metastability with clock domain crossing.	*CO2*	*PO2*	**08**

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