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B. M. S. College of Engineering, Bengaluru - 560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC5PE2OS **Max Marks: 100**
Course: Operating System **Date: 19.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1. a) What is multiprogramming system? Explain the features which supports architecture of multiprogramming system. **10**

   b) A system has 4 active processes P1, P2, P3, P4; having the following time characteristics **10**

Processes	P1	P2	P3	P4
t_c	5ms	10ms	20ms	25ms
t_{io}	15ms	5ms	25ms	20ms

   Draw a timing chart for a system when
   (a) CPU-bound programs have a higher priority
   (b) I/O-bound programs have a higher priority.

UNIT - II

2. a) Discuss the advantages of thread model over process **06**

   b) Write a Linux C program, to create a child process. Both the parent and child should print their Process ids. Let the child process execute "execlp()" to list out the file names in the current working directory. Interpret the results. **06**

   c) For a real time satellite data logging system, interpret how computation speedup is achieved by including child processes in the program. **08**

OR

3. a) Explain the attributes of Process Control Block with the relevant fields **10**

   b) Discuss the structure of hybrid thread models with different associations. **10**

UNIT - III

4. a) For an airline reservation system module, analyze how critical section can be used to avoid Race Condition. **08**

b) Assume four processes waiting in the ready queue. Find the schedule based on preemptive Shortest Time to Go (STG) algorithm and calculate the average and weighted average turnaround time. Consider the time slice as 2 units of time. Identify the instants of context switching in the schedule. **12**

Process	P1	P2	P3	P4
Admission Time	0	2	3	5
Execution	5	3	7	3

OR

5. a) Assume four processes waiting in the ready queue. Find the schedule based on non-preemptive HRN algorithm and calculate the average and weighted average turnaround time. **08**

Process	P1	P2	P3	P4
Admission time	0	1	4	2
Execution time	5	3	10	4

b) Assume four processes waiting in the ready queue. Find the schedule based on preemptive Round Robin algorithm and calculate the average and weighted average turnaround time. Consider the time slice as 2 units of time. Identify the instants of context switching in the schedule. **12**

Process	P1	P2	P3	P4
Admission time	0	2	3	5
Execution time	5	3	7	3

UNIT - IV

6. a) Discuss the memory management of memory hierarchy with different levels. **06**

b) Consider a system generating 32-bit logical address and having 128MB of main memory. Using paging scheme, page size is of 4KB. If page 200 exists in page frame 50 and byte number 100 is to be traced, show the logical and physical addresses using its address translation mechanism. **08**

c) Consider 6 consecutive memory blocks of sizes 30B-F, 40B-A, 20B-A, 50B-F, 40B-A & 60B-F (A-allocated, F-free). With free list representation, demonstrate the typical merging of memory using boundary tags when each allocated block goes free individually. **06**

UNIT - V

7. a) What are device drivers, explain the logical positioning of device drivers with neat diagram. **10**

b) Discuss the user space I/O software with layers of the I/O system and main functions of each layer. **10**

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