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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC5PCDCT **Max Marks: 100**
Course: Digital Communication Theory

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Explain the following line codes for 110101101 i) Unipolar RZ & NRZ ii) polar RZ & NRZ iii) Bipolar RZ &NRZ	*CO1*	*PO1*	**06**
	b)	Consider an audio signal consisting of the sinusoidal term given as x (t) =3cos (500πt) i). Show and determine the SQNR ratio. When this is quantized using 10 bits PCM. ii). How many bits of quantization are needed to achieve a SNR ratio of at least 40dB?	*CO1*	*PO1*	**07**
	c)	Explain how Eye Patterns can be used to Monitor the performance of PAM Systems	-	-	**07**
		OR			
2	a)	Show that the use of A law companding provides a ratio of maximum step size to minimum step size equal to the parameter A	*CO1*	*PO1*	**06**
	b)	Write the differences between PCM, DPCM	*CO1*	*PO1*	**06**
	c)	Explain the limitation of ideal solution to over come the effect of ISI in baseband transmission and what is the practical solution to solve this problem.	*CO1*	*PO1*	**08**
		UNIT - II			
3	a)	Discuss the properties of matched filter	-	-	**06**
	b)	The bit stream 1011100011 is to be transmitted using DPSK. Determine the encoded sequence and transmitted Phase sequence. Assume the reference bit to be '1' and the logic gate as Ex-NOR	*CO1*	*PO1*	**06**
	c)	Draw the block diagram of QPSK transmitter and receiver and explain the operation along with substantial Mathematical expression.	*CO1*	*PO1*	**08**
		OR			
4	a)	The bit steam (10010011) is differentially encoded and transmitted using DPSK Modulator. Assuming the reference bit as a '1' i) Design the DPSK modulator and demodulator structure and ii) Indicate the transmitted DPSK phase values.	*CO3*	*PO3*	**06**

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	b)	Draw the waveform for the binary data sequence 101100 Modulated using FSK and PSK.. Compare the probability of error of PSK with that of FSK .What is the Bandwidth requirement if the BPSK signal modulated with a carrier frequency of 140MHz modulated by data bits at a rate of 2400bits/sec	*CO1*	*PO1*	**06**
	c)	Discuss in brief Non-coherent detection of binary FSK. A binary frequency shift keying system employs two signaling frequencies 1f and 2f. The lower frequency 1f is 1200 Hz and signaling rate is 500 Baud. Calculate 2f. ?	*CO1*	*PO1*	**08**
		UNIT - III			
5	a)	State the advantages of DSSS..Compare DSSS with FHSS	*CO1*	*PO1*	**10**
	b)	Discuss frequency hop spread spectrum technique. An FHSS system employs a total bandwidth of 400 MHz and an individual channel bandwidth of 100Hz. What is the minimum number of PN bits required for each hop?	*CO1*	*PO1*	**10**
		UNIT - IV			
6	a)	Consider 4 message having probability $P_1=P_4=1/8$ and $P_2=P_3=3/8$. Calculate the entropy 'H' and information rate 'R' at the source if r=1message /sec. Write the definition of entropy.	*CO1*	*PO1*	**06**
	b)	Consider a source s={S_1 S_2} with probabilities 3/4 and 1/4 respectively. Obtain Shannon Fano code for Source S its 2nd extension and 3rd extension. Calculate the efficiency for each case.	*CO1*	*PO1*	**10**
	c)	State Shannon's Channel Capacity Theorem ? A voice grade channel of the telephone network has a bandwidth of 3.4KHz. Calculate the capacity of the telephone Channel for Signal to Noise ratio of 30dB	*CO1*	*PO1*	**04**
		UNIT - V			
7	a)	A generator matrix for a (6, 3) block code is given below $\begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 \end{bmatrix}$ a)List all the valid code vectors. b)Find out minimum distance & weight of the code. c) How many errors can be detected &corrected? d) State your observation on the result obtained. e)If the received vector R=[r_1 r_2 r_3 r_4 r_5 r_6], Design the syndrome calculating circuit	*CO3*	*PO3*	**10**
	b)	Consider the (3, 1, 2) Convolutional code with $g^{(1)}$=(110) $g^{(2)}$=(101) and $g^{(3)}$=(111) a) Design the encoder block. b) Find the generator matrix. c) Find the code word corresponding to the information sequence (11101)using time domain and transform domain approach.	*CO3*	*PO3*	**10**

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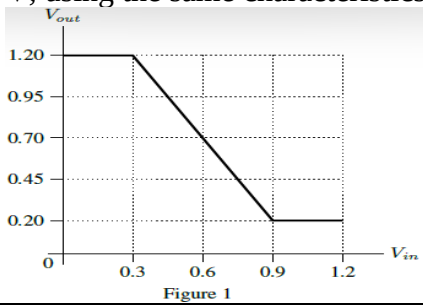
May 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC5PCFOV **Max Marks: 100**
Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	An nMOS transistor has a threshold voltage of 0.4 V and a supply voltage of V_{DD} =1.2 V. A circuit designer is evaluating a proposal to reduce V_t by 100 mV to obtain faster transistors. a) By what factor would the saturation current increase (at $V_{gs} = V_{ds} = V_{DD}$) if the transistor were ideal? b) By what factor would the subthreshold leakage current increase at room temperature at V_{gs} = 0? Assume n = 1.4. c) By what factor would the subthreshold leakage current increase	CO2	PO2	**06**
	b)	Express Gate capacitances in terms of intrinsic capacitances of a MOS gate capacitance model with necessary equations	CO1	PO1	**08**
	c)	Explain body effect in detail with relevant equation and diagram?	-	-	**06**
		UNIT - II			
2	a)	Design the CMOS circuit and Stick/layout for the given equation and mention the lambda-based design rules on layout and estimate the area. $Y = \overline{(A + B + C).D}$	CO3	PO3	**12**
	b)	Explain the process of Photolithography and importance of carbon nanotubes in VLSI.	-	-	**08**
		UNIT - III			
3	a)	Analyse the graph and determine the noise margins for the inverter whose DC characteristics is shown in Figure 1. Also estimate the output voltage of the circuit in Figure 2 if the input voltage is 0.45 V, using the same characteristics.  Figure 1  Figure 2	CO2	PO2	**06**

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		b)	Design XOR and NOR gates using transmission gates.	CO3	PO3	**06**
		c)	Design the tristate buffer, tristate inverter and 2:1 transmission gate multiplexer with neat circuit diagram.	CO3	PO3	**08**
			OR			
	4	a)	Design an AOI based clocked NAND- JK Latch and implement the same using CMOS circuit. With a truth table, Illustrate its operation.	CO3	PO3	**10**
		b)	Design a CMOS Inverter and elaborate the DC Characteristics of a CMOS Inverter at different operating conditions?	CO3	PO3	**10**
			UNIT - IV			
	5	a)	For each of the following sequencing styles, determine the maximum logic propagation delay available within a 500ps clock cycle. The clock skew between any two elements can be up to 50 ps and no-time borrowing takes place. (i) Flip-flops. (ii) Two-phase transparent latches. **Setup Time** | ***clk*-to-*Q* Delay** | ***D*-to-*Q* Delay** | **Contamination Delay** | **Hold Time** Flip-Flops: 65 ps | 50 ps | n/a | 35 ps | 30 ps Latches: 25 ps | 50 ps | 40 ps | 35 ps | 30 ps	CO1	PO1	**10**
		b)	With neat circuit diagram describe the operation of sub array architectures of DRAM.	CO1	PO1	**10**
			OR			
	6	a)	With proper circuit and timing diagrams explain the min delay of a Flip Flop and max delay constraints with respect to 2-phase transparent latches.	CO2	PO2	**10**
		b)	Illustrate, with the help of neat circuit diagram and relevant waveforms, the read and write operations of a six transistor SRAM cell.	CO1	PO1	**10**
			UNIT - V			
	7	a)	Explain BIST testing with respect to pseudo random sequence generator and 3-bit register used in DFT.	-	-	**10**
		b)	Illustrate the various fault models under manufacturing test principles in DFT.	CO1	PO1	**10**

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May 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC5PE1OS **Max Marks: 100**
Course: Operating System

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Briefly explain the different classes of operating system, specifying the primary concern and key concepts used.	*CO1*	*PO1*	**10**
	b)	In a timesharing system Processes *P*1 and *P*2 follow a cyclic behavior pattern. Each cycle contains a burst of CPU activity to service a subrequest and a burst of I/O activity to report its result, followed by a wait until the next subrequest is submitted to it. The CPU bursts of processes *P*1 and *P*2 are 10 and 30 ms, respectively, while the I/O bursts are 80 and 60 ms, respectively. Illustrate the operation by drawing a timing chart. Find the response time of the processes assuming the time slice to be 10ms.	*CO1*	*PO1*	**10**
		UNIT - II			
2	a)	Explain the fundamental state transition for a process with state transition diagram.	*CO2*	*PO2*	**10**
	b)	Differentiate kernel level threads and user level threads.	*CO2*	*PO2*	**10**
		UNIT - III			
3	a)	Define dead lock. Discuss the condition of a dead lock in resource allocation.	*CO2*	*PO2*	**10**
	b)	Implement Round robin scheduling with a time slices of 6 milli seconds for the processes listed in the table 2, find the average waiting time. Table 2 Processes for Scheduling	*CO2*	*PO2*	**10**

Process	P1	P2	P3
Service time	24	3	3

		OR			

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<table>
<tr><td></td><td>4</td><td>a)</td><td>For the following set of process perform FCFS & SRN scheduling. calculate mean turn-around time and mean weighted turn around
<table><tr><td>process</td><td>P_1</td><td>P_2</td><td>P_3</td><td>P_4</td><td>P_5</td></tr><tr><td>Admission time</td><td>0</td><td>2</td><td>3</td><td>4</td><td>8</td></tr><tr><td>Service time</td><td>3</td><td>3</td><td>5</td><td>2</td><td>3</td></tr></table></td><td>CO2</td><td>PO2</td><td>10</td></tr>
<tr><td></td><td></td><td>b)</td><td>Explain the three main approaches to real-time scheduling.</td><td>CO2</td><td>PO2</td><td>10</td></tr>
<tr><td></td><td></td><td></td><td>UNIT - IV</td><td></td><td></td><td></td></tr>
<tr><td></td><td>5</td><td>a)</td><td>Explain non-contiguous memory allocation to process ‘p’ with neat diagram.</td><td>CO2</td><td>PO2</td><td>10</td></tr>
<tr><td></td><td></td><td>b)</td><td>Differentiate paging and segmentation with example.</td><td>CO2</td><td>PO2</td><td>10</td></tr>
<tr><td></td><td></td><td colspan="2">OR</td><td></td><td></td><td></td></tr>
<tr><td></td><td>6</td><td>a)</td><td>Differentiate three-page replacement policies with example.</td><td>CO2</td><td>PO2</td><td>10</td></tr>
<tr><td></td><td></td><td>b)</td><td>Consider the page reference string 5,4,3,2,1,4,3,5,4,3,2,1,5. Calculate the page faults using FIFO & LRU page replacement policies with a frame size 3.</td><td>CO2</td><td>PO2</td><td>10</td></tr>
<tr><td></td><td></td><td></td><td>UNIT - V</td><td></td><td></td><td></td></tr>
<tr><td></td><td>7</td><td>a)</td><td>Correlate File system and IOCS.</td><td>CO3</td><td>PO2</td><td>10</td></tr>
<tr><td></td><td></td><td>b)</td><td>Discuss the implementation of file operations by IOCS.</td><td>CO3</td><td>PO2</td><td>10</td></tr>
</table>

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B.M.S.College of Engineering, Bengaluru-560019

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May 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: V**
Branch: ES Cluster (EI/EC) **Duration: 3 hrs.**
Course Code: 22ES5PCDSP **Max Marks: 100**
Course: Digital Signal Processing

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.
3. Use Filter Table if needed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Compute the 4-point DFT of the sequence x(n) = cos(πn)	CO1	PO1	**06**
	b)	Find the DFT of the sequence x[n]={1, 1, -1, -1} and also find the DFT of x[(n-2)mod4] by definition and verify the result using circular shift property	CO1	PO1	**07**
	c)	Find the Circular Convolution for the following sequences for N=8 $x_1(n)$={1, 0, 1, 0, 1, 0, 1, 1 } $x_2(n)=\cos(2\pi/3)n$ for $0\leq n\leq 7$	CO1	PO1	**07**
		OR			
2	a)	Compute the N-point DFT of each of the following sequence i) $x(n)=\delta(n)$ ii) $x(n)=\delta(n-n_0)$ where $0<n_0<N$ iii) $x(n)=a^n$ $0\leq n\leq N$ iv) $x(n)=u(n)-u(n-n_0)$ where $0<n_0<N$	CO1	PO1	**08**
	b)	Find the DFT of the given Sequence, $x(n)=1 \quad n-even$ $=0 \quad n-odd$	CO1	PO1	**06**
	c)	Given $x_1(n)$={1, -1, 1} and $x_2(n)$ ={ 2, 2, 2} Compute the linear convolution using circular convolution.	CO1	PO1	**06**
		UNIT - II			
3	a)	Determine the output y(n) of a filter whose impulse response is h(n)={1, 1, 1} and input signal x(n)={3,-1,0,1,3,2,0,1,2,1} using using i) Overlap Save Method ii) Overlap Add Method Use Block Length N=5	CO1	PO1	**10**

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		b)	Find 8 point DFT of the sequence using DIT-FFT algorithm X(n)={ ½, ½, ½, ½, 0, 0, 0, 0 } Analyze the reduction in number of computations in DIT-FFT as compared to direct computation of DFT	*CO2*	*PO2*	**10**
			UNIT - III			
	4	a)	For the given specification α_p=3 dB, α_s=15 dB; Ω_p=1000 rad/sec and Ω_s=500 rad/sec. Design a digital high pass filter. Use Butter worth Polynomial to obtain H(s) and Bilinear Transformation Technique to obtain H(z). T=1s	*CO3*	*PO3*	**10**
		b)	The system function of the analog filter is given as $H_a(S) = \frac{S+0.1}{(S+0.1)^2+9}$ Obtain the system function of the IIR digital filter by using impulse variance method. Comment on Stability	*CO2*	*PO2*	**10**
			OR			
	5	a)	Obtain a cascade realization for a system described by $H(z) = \frac{1+\frac{1}{4}Z^{-1}}{(1+\frac{1}{2}Z^{-1})(1+\frac{1}{2}Z^{-1}+\frac{1}{4}Z^{-2})}$	*CO1*	*PO1*	**08**
		b)	Design a digital low pass filter of -3dB cut off at 500 Hz and attenuation at -15 dB at 750 Hz and sampling rate =2000 samples per second, using Bilinear Transformation Technique.	*CO3*	*PO3*	**12**
			UNIT - IV			
	6	a)	A low pass filter is to be designed with the following desired frequency response $H_d(e^{j\omega}) = \begin{cases} e^{-j2\omega}, & \lvert\omega\rvert < \frac{\pi}{4} \\ 0 \quad , & \frac{\pi}{4} < \lvert\omega\rvert < \pi \end{cases}$ Determine the filter coefficients $h_d(n)$ if the window function is defined as $\omega(n) = \begin{cases} 1 & 0 \le n \le 4 \\ 0 & otherwise \end{cases}$ Also determine the frequency response $H(e^{j\omega})$ of the desired filter, Magnitude and Phase response of $H(e^{j\omega})$	*CO3*	*PO3*	**10**
		b)	Design a lowpass FIR Filter using frequency sampling technique using cutoff frequency of π/2 rad/sec. The filter should have linear phase and length of 17.	*CO3*	*PO3*	**10**

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			UNIT - V			
	7	a)	Explain the application of adaptive filtering to system modeling.	*CO1*	*PO1*	**07**
		b)	Describe the adaptive Noise cancelling system with a neat diagram.	*CO1*	*PO1*	**07**
		c)	Given a DSP upsampling system with the following specifications: Sampling rate =6000 Hz, Input audio frequency range=0-800 Hz, passband ripple=0.02 dB, Stopband attenuation =50 dB, upsample factor L=3. Determine the FIR filter length, cut off frequency and window type if window design method is used.	*CO1*	*PO1*	**06**

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