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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC5PCFOV **Max Marks: 100**
Course: Fundamentals of VLSI **Date: 01.03.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Discuss the VLSI design flow with appropriate diagrams. Also illustrate each step with an appropriate example. **08**

b) Explain the C-V characteristics of MOSFET in the different regions of operation. **06**

c) Explain velocity saturation and channel length modulation with neat diagrams and necessary equations. **06**

UNIT - II

2 a) Explain n-well fabrication process with appropriate sketches to build a CMOS inverter. **10**

b) Apply the design rules to build a layout that realizes the following Boolean expression (constructing the layout with minimum height) and estimate the cell height and width in terms of λ. **06**

Note: Don't simplify the expression.

$$Y = \overline{(A + B + C) \cdot D}$$

c) Differentiate between wet and dry oxidation. **04**

OR

3 a) What are layout design rules? Explain the basic λ-based design rules? Design a minimum-sized inverter layout based on the rules mentioned above. Also calculate the area for the inverter layout. **10**

b) With a neat sketch, explain LDD structure. **06**

c) Write the difference between positive and negative photoresist. **04**

UNIT - III

4 a) Derive the DC characteristics for a CMOS inverter. Highlight the different regions of operation for the same when the input changes from 0 to V_{DD}. Also plot I_{DSN}/I_{DSP} vs V_{DD}, given V_{DD}= 5V, Vtn=|Vtp|=1.5V. **10**

b) Find the mode of operation (cutoff, linear, or saturation) and drain current I_D for the applied bias V_{GS} = 1.5V, V_{DS} = 1.5V with V_{SB}= 0.5V for an NMOS transistor; given V_{t0} = 0.7V, W/L = 4/1, γ= 0.35V, λ= 0.05 V^{-1}, μC_{ox} = 350 $\mu A/V^2$, and Φ_s = 0.6 V. **04**

c) Design 4:1 multiplexer and XOR gate using Transmission gates. **06**

UNIT - IV

5 a) Briefly explain the operation of CMOS implementation of a negative edge triggered master slave D flip-flop. **05**

b) Realize CMOS clocked JK latch based on AOI implementation. **05**

c) Obtain the maximum delay constraints for the combinational logic delay when a combinational logic is sequenced with the following sequencing elements: **10**
i. Flip-Flop
ii. Two phase transparent latches
iii. Pulsed latches

OR

6 a) Obtain the Minimum delay constraint for the combinational logic delay, with the help of appropriate timing diagram, when sequenced with the following sequencing elements: **10**
i. Flip-flop
ii. Two phase transparent latches
iii. Pulsed latches

b) For each of the following sequencing styles, determine the minimum logic contamination delay in each clock cycle (or half-cycle, for two-phase latches). **10**
i) Flip-Flops
ii) Two-phase transparent latches with 50% duty cycle clocks
iii) Two-phase transparent latches with 60 ps of non-overlap between phases
iv) Pulsed latches with 80 ps pulse width
The particulars of the flip-flops and latches used are given in Table 1.

Table 1: Question 6.(b)

	Setup time	clk-to-Q delay	D-to-Q delay	Contamination delay	Hold time
Flip-flops	65 ps	50 ps	n/a	35 ps	30 ps
Latches	25 ps	50 ps	40 ps	35 ps	30 ps

UNIT - V

7 a) Using 6T SRAM cell and appropriate waveforms, explain the Read and Write operations. Also discuss the constraints during the read and write operation. **10**

b) Realize a 4-word by 6-bit ROM using pseudo-nMOS pull-ups with the following contents: **06**
word0: 010101
word1: 011001
word2: 100101
word3: 101010

c) Draw 1 T DRAM cell and explain its write and read operations. **04**

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