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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC5PCFOV **Max Marks: 100**
Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1	a)	Discuss the various design abstractions in VLSI design with the help of the Gajski Y-chart.	**10**
	b)	Briefly discuss the following non-idealities in I-V characteristics of MOS devices: (i) velocity saturation and (ii) body effect.	**06**
	c)	An nMOS transistor has a threshold voltage of 0.45 V and a supply voltage of V_{DD} = 1.2 V. A circuit designer is evaluating a proposal to reduce V_t by 100 mV to obtain faster transistors. By what factor would the sub-threshold leakage current increase at room temperature at V_{gs} = 0? Assume n = 1.4.	**04**

OR

2	a)	Illustrate the CMOS process flow for formation of NFET & PFET on a substrate material starting from epitaxial layer using masks.	**10**
	b)	Analyse with the help of graph the behaviour of intrinsic MOS gate capacitance as a function of a Vgs and Vds of a MOS capacitance.	**10**

UNIT - II

3	a)	With the help of neat diagrams, explain the process of photolithography used to pattern a layer of polysilicon in the semiconductor manufacturing process.	**07**
	b)	Discuss any two CMOS process enhancements briefly.	**06**
	c)	With the help of λ-based design rules, estimate the area of a 3-input NOR gate.	**07**

OR

4	a)	Design a CMOS circuit and stick diagram to realize the Boolean function $F = \overline{X + YZ + XYZ}$ using the minimum number of transistors possible. Also find the area estimate of the layout pattern thus drawn.	**09**
	b)	With the help of neat diagrams, discuss the fabrication of a CMOS inverter starting from a silicon wafer.	**11**

UNIT - III

5 a) With the help of relevant diagrams, discuss the DC characteristics of a CMOS inverter. **10**

b) Design a two-input NAND gate using transmission gates. **06**

c) The output of an nMOS transistor is used to drive the gate of another nMOS transistor as shown in Figure 1. Given: V_{DD} = 3.3 V, V_t = 0.4 V. Find the output voltage V_{out} when the input voltages are at the following values: **04**

i. V_a = 2.0 V and V_b = 2.5 V

ii. V_a = 3.3 V and V_b = 1.8 V

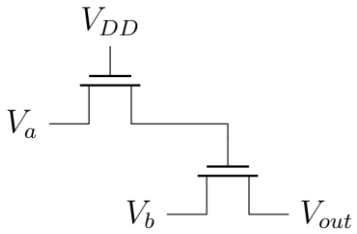

Figure 1: Question 4.(c)

OR

6 a) Design a 4:1 MUX using 2:1 MUX implemented by a tristate inverter and realize an XOR function using transmission gate. **10**

b) Highlight the significance of noise margin in a CMOS. An inverter has the transfer characteristics shown in Figure 2. Determine the values of V_{IL}, V_{IH}, V_{OL}, and V_{OH} .Find the noise margin (Assume suitable values from within range). **10**

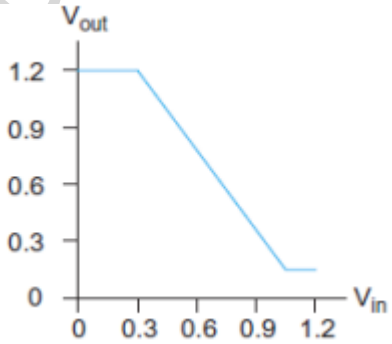

Figure 2: Question 6.(b)

UNIT - IV

7 a) With the help of neat diagrams, discuss the operation of a bistable element. **08**

b) Establish the relevance for master-slave JK flip flop; and explain its construction and working with the help of relevant circuit diagrams. **08**

c) Demonstrate the realization of a D-latch using tristate inverters. **04**

OR

8 a) Briefly describe the three methods of sequencing combinational circuits. **09**

b) Establish the Min-delay constraints in the context of a flip-flop. **05**

c) Briefly explain the concept of time borrowing with a neat illustration. **06**

UNIT - V

9 a) Explain the read and write operation in a 6 transistor SRAM cell with the help of neat diagrams. **10**

b) Briefly describe the construction and operation of dynamic RAM with neat diagrams. **06**

c) With the help of a block diagram of NAND ROM, mention one disadvantage and one advantage with NAND ROM. **04**

OR

10 a) Explain DRAM subarray architecture with relevant diagrams. **10**

b) Explain the trade-offs between open, folded and twisted bit-lines in dynamic RAM arrays **10**

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