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B. M. S. College of Engineering, Bengaluru - 560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC5PCFOV **Max Marks: 100**
Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1. a) Derive the long channel I-V characteristics of a MOSFET with proper equations. **08**

   b) Explain the mobility degradation and velocity saturation with proper equations and graphs. **08**

   c) Write a short note on Body effect. **04**

UNIT - II

2. a) Briefly explain all the steps in CMOS fabrication process. **10**

   b) Draw the CMOS circuit and Stick diagram for the equation $Y = \overline{(A+B).C}$ **06**

   c) Write a Short note on Carbon Nano Tubes. **04**

OR

3. a) Explain Photolithography process with neat diagram. **04**

   b) Draw the CMOS circuit, CMOS stick diagram and CMOS layout for the given expression. **10**

$$Y = \overline{(AB+CD).E}$$

   c) Write a Short note on: **06**

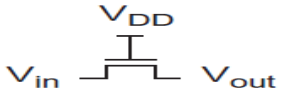
   (1) Silicon on Insulator (SOI).

   (2) Differentiate LOCUS and STI method.

UNIT - III

4. a) Suppose VDD=1.8V & Vt=0.6V. Find the output voltage for the following. **06**

   i) Vin=0V. ii) Vin=0.7V. iii) Vin=1.2V. iv) Vin=1.6V.



   b) Explain beta ratio effects with proper expressions and characteristics. **06**

   c) Explain tristate buffer, tristate inverter and 2:1 transmission gate multiplexer with neat circuit diagram. **08**

UNIT - IV

5. a) Design an AOI based NOR SR-Latch and implement the same using CMOS Circuit. With truth table, Illustrate its operation. **10**

   b) Analyse the given Design sequencing styles to determine the minimum logic contamination delay in each clock cycle (or half-cycle, for two-phase latches). Assume there is 20ps clock skew. (i) Flip-flops. (ii) Two-phase transparent latches with 50% duty cycle clocks. (iii) Two-phase transparent latches with 40 ps of nonoverlap between phases. (iv) Pulsed latches with 80 ps pulse width. **10**

	Setup Time	*clk*-to-*Q* Delay	*D*-to-*Q* Delay	Contamination delay	Hold Time
Flip-Flops	65 ps	50 ps	n/a	35ps	30 ps
Latches	25ps	50ps	40ps	25ps	30ps

OR

6. a) Design an AOI based clocked NAND- JK Latch and implement the same using CMOS circuit. With a truth table, Illustrate its operation. **10**

   b) For each of the following sequencing styles, determine the maximum logic propagation delay available within a 400ps clock cycle. The clock skew between any two elements can be up to 40 ps and no-time borrowing takes place. **10**

   (i) Flip-flops. (ii) Two-phase transparent latches. (iii) Pulsed latches with 70 ps pulse width.

	Setup Time	*clk*-to-*Q* Delay	*D*-to-*Q* Delay	Contamination Delay	Hold Time
Flip-Flops	65 ps	50 ps	n/a	35 ps	30 ps
Latches	25 ps	50 ps	40 ps	35 ps	30 ps

UNIT - V

7. a) With neat illustrations, discuss the Read and Write operation on a 6-transistor SRAM Cell. **10**

   b) Design 4-word by 6-bit ROM using pseudo-nMOS pull-ups with the following contents. Sketch DOT diagram for the same. **10**

   Word 0: 010101; Word 1: 011001; Word2: 100101; Word 3: 101010

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