U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

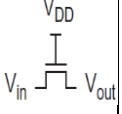
Autonomous Institute Affiliated to VTU

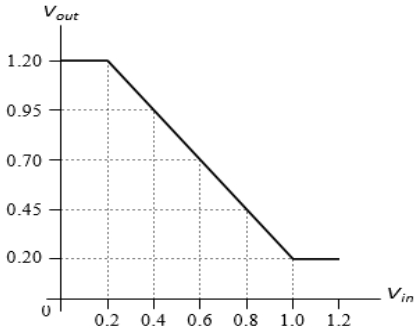
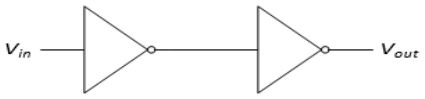
July 2024 Semester End Main Examinations

Programme: B.E. **Semester: V**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC5PCFOV **Max Marks: 100**
Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

				CO	*PO*	Marks
			UNIT - I			
1	a)	Derive the long channel I-V characteristics of a MOSFET with neat diagram.		CO2	PO2	**08**
	b)	Analyze with a suitable graph, the behavior of intrinsic MOS capacitance as a function of : a. V_{GS} b. V_{DS}		CO2	PO2	**08**
	c)	Write a short note on channel length modulation?		-	-	**04**
		UNIT - II				
2	a)	Describe the fabrication of CMOS inverter using n-well process with neat diagram.		CO1	PO1	**10**
	b)	Design the CMOS circuit and stick diagram for the equation $Y = \bar{A}.B + C.\bar{D}$		CO3	PO3	**06**
	c)	Write a Short note on FinFETs.		-	-	**04**
		UNIT - III				
3	a)	Suppose VDD=1.8V & Vt=0.6V. Find the output voltage for the following. i) Vin=0V. ii) Vin=0.7V. iii) Vin=1.2V. iv) Vin=1.6V.		CO2	PO2	**06**

		b)	Analyze the graph and determine the noise margins for the inverter whose DC characteristics is as shown in Figure 1. Also estimate the output voltage of the circuit in Figure 2 if the input voltageis 0.4 V, using the same characteristics.  Figure 1  Figure 2	CO2	PO2	**06**
		c)	Design a tristate inverter and 2x1 multiplexer using transmission gates.	CO3	PO3	**08**
			OR			
	4	a)	Design 2 input XOR and 2 input NAND gates using transmission gates.	CO3	PO3	**05**
		b)	Analyze the DC Characteristics of a CMOS Inverter indicating the various regions of operations.	CO2	PO2	**07**
		c)	Design an AOI based clocked NAND- JK Latch and implement the same using CMOS circuit and illustrate its operation.	CO3	PO3	**08**
			UNIT - IV			
	5	a)	Analyse the given design sequencing styles to determine the minimum logic contamination delay in each clock cycle (or half-cycle, for two-phase latches). Assume there is zero clock skew. (i) Flip-flops. (ii) Two-phase transparent latches with 50% duty cycle clocks. (iii) Two-phase transparent latches with 60 ps of nonoverlap between phases. <table><tr><th></th><th>Setup Time</th><th>*clk*-to-*Q* Delay</th><th>*D*-to-*Q* Delay</th><th>Contamination delay</th><th>Hold Time</th></tr><tr><td>Flip-Flops</td><td>65 ps</td><td>50 ps</td><td>n/a</td><td>35ps</td><td>30 ps</td></tr><tr><td>Latches</td><td>25ps</td><td>50ps</td><td>40ps</td><td>25ps</td><td>30ps</td></tr></table>	CO2	PO2	**10**
		b)	With neat illustrations, discuss the Read and Write operation on a 6-transistor SRAM Cell.	CO2	PO2	**10**
			OR			
	6	a)	Illustrate the min delay and max delay constraints with respect to flip flops and 2-phase transparent latches with relevant timing diagrams.	CO2	PO2	**10**

		b)	Implement the sub array architectures of DRAM and describe its operation.	CO2	PO2	**10**
			UNIT - V			
	7	a)	Illustrate Adhoc testing and parallel scan based testing in DFT technique.	CO2	PO2	**10**
		b)	Write a short note of the following: i) ATPG. ii) Boundary Scan	-	-	**10**

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