U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 23EC5PCFOV / 22EC5PCFOV **Max Marks: 100**

Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

				CO	PO	Marks
			UNIT - I			
1	a)		Illustrate PMOS and NMOS as a switch with switch level models	*CO 1*	*PO 1*	**6**
	b)		Implement a 3 Input NAND GATE and NOR GATE using CMOS logic.	*CO 1*	*PO 2*	**6**
	c)		With suitable graphs illustrate the various types of intrinsic MOS Capacitance models	*CO 1*	*PO 2*	**8**
			OR			
2	a)		Illustrate the effect of channel length modulation in a MOSFET.	*CO 1*	*PO 2*	**6**
	b)		Highlight the significance of subthreshold leakage in MOSFETs	*CO 1*	*PO 2*	**6**
	c)		Deduce an expression for drain current in long channel MOSFETS	*CO 1*	*PO 2*	**8**
			UNIT - II			
3	a)		Illustrate, with the help of neat diagrams, the process by which a given layer in the planar CMOS fabrication technology can be patterned as desired. Also discuss the difference between positive and negative photoresist.	*CO 1*	*PO 1*	**10**
	b)		Implement the gate level and stick diagram for the function $Y=\overline{(A+B+C)\cdot D}$ using CMOS logic. Also estimate the cell width and height.	*CO 2*	*PO 2*	**10**
			OR			
4	a)		Discuss in detail, the λ-based design rules with neat illustrations.	*CO 1*	*PO 1*	**10**
	b)		Implement a 2:1 Mux using transmission gates.	*CO 2*	*PO 2*	**10**

			UNIT - III			
	5	a)	Deduce the DC transfer function for a static CMOS Inverter.	***CO 2***	***PO 1***	**10**
		b)	Implement a SR latch based NOR gates.	***CO 3***	***PO 3***	**10**
			OR			
	6	a)	What is noise margin? Obtain an expression for N_{ML} and N_{MH} from transfer characteristics of inverter.	***CO 2***	***PO 1***	**10**
		b)	Show the implementation of a D latch using a tristate buffer.	***CO 3***	***PO 3***	**10**
			UNIT - IV			
	7	a)	Illustrate the static sequencing techniques with relevant timing diagrams and highlight its significance.	***CO 2***	***PO 2***	**10**
		b)	"In the system using transparent latches, clock skew does not degrade performance." Justify the statement.	***CO 2***	***PO 2***	**10**
			OR			
	8	a)	Suggest and describe a suitable design to implement noise sources for hold margin,	***CO 2***	***PO2***	**10**
		b)	Illustrate the concept of time borrowing with a suitable example.	***CO 2***	***PO 2***	**10**
			UNIT - V			
	9	a)	Highlight the significance of silicon debug principles. Classify the same.	***CO 1***	***PO1***	**10**
		b)	Describe the struck at zero and struck at one faults for effective fault detection in transistors.	***CO 1***	***PO1***	**10**
			OR			
	10	a)	Highlight the importance of Shmoo plots in failure analysis. Analyze the various probabilities of failures using Shmoo plots,	***CO 1***	***PO1***	**10**
		b)	Briefly describe the methods to verify proper functionality using BIST.	***CO 1***	***PO1***	**10**

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