U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 23EC5PCFOV / 22EC5PCFOV **Max Marks: 100**

Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Derive a model relating the current and voltage (I-V) for an nMOS transistor in each regions.	*CO 1*	*PO1*	**10**
	b)		Discuss the detailed MOS capacitance model with relevant equations and graph?	*CO 1*	*PO 1*	**10**
			OR			
2	a)		Represent a 3 input CMOS NOR gates and describe it's working.	*CO 1*	*PO 1*	**6**
	b)		Discuss in detail the partitioning of Digital VLSI design in different levels of abstractions.	*CO 1*	*PO 1*	**8**
	c)		Describe in detail the working principle of CMOS logic gate.	*CO 1*	*PO 1*	**6**
			UNIT - II			
3	a)		Describe the Well and Channel Formation in CMOS technologies with a neat diagram.	*CO 2*	*PO 1*	**10**
	b)		Analyse the λ based design rules and guidelines involved in CMOS layout .	*CO 2*	*PO 2*	**10**
			OR			
4	a)		Analyse the different design rules used to build reliably functional circuits.	*CO 2*	*PO 2*	**10**
	b)		Describe the CMOS fabrication process.	*CO 2*	*PO 1*	**10**
			UNIT - III			
5	a)		Analyse the DC transfer characteristics of a CMOS inverter highlighting all the different regions of operation.	*CO 2*	*PO 2*	**10**
	b)		Illustrate the operation of the Pass transistor logic structures with suitable examples highlighting their threshold drop.	*CO 2*	*PO 2*	**10**

			OR			
	6	a)	Propose a suitable two phase clocking strategy for any sequential circuit and analyse the working of the same.	*CO 2*	*PO 2*	**10**
		b)	Illustrate the working of a Simple CMOS SR Latch with the block diagram.	*CO 2*	*PO 2*	**10**
			UNIT - IV			
	7	a)	Illustrate with the diagram the circuit structure and the operation of simple SRAM cells.	*CO 2*	*PO 2*	**10**
		b)	Design a four-transistor resistive-load SRAM cell with read and write operation with waveform.	*CO 3*	*PO 3*	**10**
			OR			
	8	a)	Illustrate the 4T DRAM cell highlighting the significance of wordline and bitline.	*CO 2*	*PO 2*	**10**
		b)	Design a DRAM Subarray Architecture using a typical subarray size of 256 words by 512 bits.	*CO 3*	*PO 3*	**10**
			UNIT - V			
	9	a)	Describe the different Faults types and Models.	*CO 1*	*PO 1*	**10**
		b)	Illustrate LFSR model and BILBO for Built in self test.	*CO 2*	*PO 2*	**10**
			OR			
	10	a)	Discuss the different models to detect the faults in DUT.	*CO 1*	*PO 1*	**10**
		b)	Illustrate the different Scan design techniques and mention the general methods for testing with the scan path approach.	*CO 2*	*PO 2*	**10**

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