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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

July 2023 Semester End Main Examinations

Programme: B.E. **Semester: VI**
Branch: ES – Cluster Elective **Duration: 3 hrs.**
Course Code: 19EC6CE1PD **Max Marks: 100**
Course: Physical Design **Date: 19.07.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			CO	**PO**	**Marks**
		UNIT - I			
1	a)	Analyze the switching characteristics of a CMOS inverter and obtain the optimal sizing ratio that minimizes the propagation delay.	*CO3*	*PO2*	**10**
	b)	Discuss the different delay models used for characterizing standard cells.	*CO1*	-	**10**
		OR			
2	a)	Demonstrate how the problems of latch-up and Electrostatic Discharge are overcome in design of Input-Output pads.	*CO2*	*PO1*	**10**
	b)	Explain the different file formats in the context of VLSI Physical Design.	*CO1*	--	**10**
		UNIT - II			
3	a)	Analyze the Polish expression PE = **25V1H374VH6V8VH** and obtain the slicing tree. Also determine the optimal floorplan using the technique of simulated annealing, given that the (width, height) of blocks 1 to 8 are respectively **{(2,4), (1,3), (3,3), (3,5), (3,2), (5,3), (1,2) (2,4)}.** Compute the change in area?	*CO3*	*PO2*	**12**
	b)	Explain Cluster growth and Hierarchical partitioning techniques.	*CO1*	--	**08**
		UNIT - III			
4	a)	Write short notes of the following: i) Global Placement. ii) Pre-placement Sanity Checks.	*CO1*	--	**08**
	b)	Discuss the simulated annealing technique for placements with an algorithm, perturb function and Timberwolf schedule function. Also explain the move restrictions with relevant equations.	*CO1*	--	**12**

			UNIT - IV			
	5	a)	Obtain the set-up and hold timing constraints for flip flop-based synchronous design in the presence of clock skew with relevant diagram and equations. Also list the methods to reduce the clock skew.	*CO2*	*PO1*	**10**
		b)	Explain the need for clock buffers with neat figure.	*CO1*	--	**04**
		c)	List the advantages and disadvantages of H-tree and X-tree.	*CO2*	*PO1*	**06**
			UNIT - V			
	6	a)	What is Electron Migration? What are the effects of EM on metal layers? Discuss the various methods to fix EM.	*CO1*	--	**10**
		b)	Explain High-tower line search algorithm to find the path between source and the target with the help of an example.	*CO1*	--	**10**
			OR			
	7	a)	Write a short note on (i) DRC (ii) LVS & (iii) ERC.	*CO1*	--	**10**
		b)	Differentiate between static and dynamic IR drop. Also specify how to fix those issues.	*CO2*	*PO1*	**05**
		c)	Briefly discuss global and detailed routing.	*CO1*	--	**05**

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