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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: VI**
Branch: ES – Cluster Elective **Duration: 3 hrs.**
Course Code: 19EC6CE1PD **Max Marks: 100**
Course: Physical Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) With a neat flow diagram, explain the ASIC Physical Design flow. **08**

b) What are standard cells? Predict the average propagation delay of a standard inverter cell and estimate the channel dimensions of the PMOS and NMOS so as to have optimum rise and fall time. **12**

OR

2 a) What are the various input files in the physical design? Discuss .lib, .lef and gdsII file in physical design. **10**

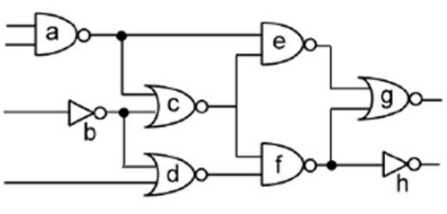
b) What is Electrostatic discharge (ESD) event? Explain the primary, secondary, power supply protection and overall protection circuit with neat diagrams. **10**

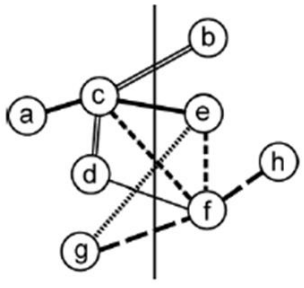
UNIT - II

3 a) Explain the difference between simulated annealing and greedy algorithm. **04**

b) Consider the following polish expression: PE = 37H51V82HV4V6VH. The (width, height) of the modules 1 through 8 are {(2,4), (1,3), (3,3), (3,5), (3,2), (5,3), (1,2), (2,4)}. Draw the initial slicing tree, its initial floorplan and estimate the total floorplan area for PE1. Assume that xHy means x is top and y is bottom, and xVy means x is left and y is right in the polish expression. Place the lower left corner of each block to the lower left corner of its room. **08**

c) For the gate level circuit shown in Fig 1(a), the graph and given an initial partition {acdg, befh} is shown in fig 1(b), calculate the gain of all cells and draw the bucket structure using FM algorithm. Perform two swaps (moves) based on the area constraint [3, 5]. **08**





UNIT - III

4 a) Explain the Timberwolf algorithm for placement. Also, discuss the steps of PERTURB function. **10**

b) For a five terminal net, the terminal coordinates are given as (5,5), (7,8), (10,12), (15,3) and (12, 15) respectively. Calculate the estimated length of net using following topologies (i) minimum chain. (ii) minimum spanning tree (iii) steiner minimum tree (iv) semi-perimeter (v) complete graph. **10**

UNIT - IV

5 a) Discuss the set-up time and hold time constraints in presence of skew with relevant diagrams and equations. Discuss the various methods to reduce clock skew? **12**

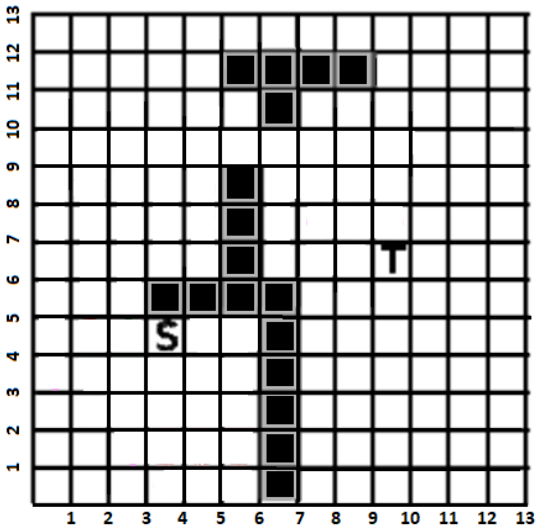
b) What are the need of clock buffers in sequential circuits? Design a buffered clock tree. **08**

UNIT - V

6 a) What is Crosstalk Analysis & Antenna Effect in Physical design? **10**

b) i. Find the path between source (S) and target (T) using Lee's algorithm (Phase 1- Filling only). Also, calculate its memory requirement. **10**

ii. Find the path between source (S) and target (T) using Hadlock's algorithm. Also, calculate the length of path connecting S and T.



OR

7 a) Discuss the Lee's algorithm for routing with an example. Explain the various steps (phases) used in Lee's algorithm. Also, describe the methods required to reduce the run time of Lee's algorithm. **10**

b) What are the various design issues in Physical design? Explain one of the issue in detail and discuss the method to reduce it. **10**

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