U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC6PE2SV **Max Marks: 100**
Course: System Verilog and Verification

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			CO	PO	Marks
		UNIT – I			
1	a)	Discuss the different types of Code coverage with examples.	*CO 1*	-	**10**
	b)	Discuss the importance of verification and analyze the cost of bugs over time.	*CO 3*	*PO2*	**10**
		OR			
2	a)	Discuss the key features of System Verilog and compare system Verilog with Verilog.	*CO 1*	-	**10**
	b)	Develop a Verilog RTL for a 3-bit counter with asynchronous reset and synchronous set inputs. Also write a test bench using interface with clocking blocks and modports.	*CO 3*	*PO2*	**10**
		UNIT – II			
3	a)	Develop the Verilog RTL for a T Flip flop with asynchronous active high reset and synchronous set and test it by developing the System Verilog Test Bench that includes interface block with clocking block and mod-ports.	*CO 4*	*PO 3*	**12**
	b)	Discuss the System Verilog event queue in detail.	*CO 1*	-	**8**
		OR			
4	a)	Develop the Verilog RTL for a D Flip flop with asynchronous active high reset and synchronous set and test it by developing the System Verilog Test Bench using interface with clocking block and mod-ports.	*CO 4*	*PO 3*	**12**
	b)	Compare packed and unpacked arrays with examples.	*CO 1*	-	**8**
		UNIT - III			
5	a)	Develop a system Verilog RTL for a 4-bit adder with clock and reset pins.	*CO 4*	*PO 3*	**8**
	b)	Develop a SV environment to randomize inputs using Transactor class for the design in 3a) and drive it to the design using driver class.	*CO 4*	*PO 3*	**12**

			OR			
	6	a)	Discuss Inheritance and Polymorphism in System Verilog with suitable examples. Also discuss overriding of methods in the subclass.	***CO 1***	-	**8**
		b)	For a 4 bit Universal shift register, develop a SV environment to randomize inputs using Transactor class and drive it to the design using driver class.	***CO 4***	***PO 3***	**12**
			UNIT – IV			
	7	a)	Using assertions, develop the System Verilog Assertion based Testbench for a divide by 16 counter and generate the assertions when i) The output count value is 9 ii) When the reset is activated	***CO 4***	***PO 3***	**12**
		b)	Discuss the benefits of assertion and also elaborate the 3 main components of concurrent assertions.	***CO 1***	-	**8**
			OR			
	8	a)	Distinguish between immediate assertions and concurrent assertions	***CO 1***	-	**8**
		b)	Develop a Verilog RTL for a 4-bit Shift register with mode control for right and left shift operations. Also a load pin is asserted for parallel loading.	***CO 4***	***PO 3***	**12**
			UNIT – V			
	9	a)	For a 4-bit Arithmetic Logic unit, develop the System Verilog test bench with the following: i) Driver Class for defining functional covergroups and coverpoints, Randomizing, driving and sampling the coverage. ii) Transactor class to define the constraint rand properties iii) Program block, Interface and Top module	***CO 4***	***PO 3***	**12**
		b)	Discuss Mailbox and the methods available in system verilog for accessing mailboxes with suitable examples.	***CO 1***	-	**8**
			OR			
	10	a)	Discuss the following with suitable examples: i) Cross coverage ii) Bins iii) Auto_bin_max iv) Transition bin v) At least()	***CO 1***	-	**10**
		b)	Discuss the following with examples: i) Cover points ii) Implicit and Explicit Bins	***CO 1***	-	**10**

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