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# B.M.S. College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## October 2024 Supplementary Examinations

**Programme: B.E.** **Semester: VI**
**Branch: Electronics and Communication Engineering** **Duration: 3 hrs.**
**Course Code: 22EC6PE2SV** **Max Marks: 100**
**Course: System Verilog and Verification**

**Instructions**: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

**Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

| | | | | CO | PO | Marks |
|---|---|---|---|---|---|---|
| | | | **UNIT – I** | | | |
| 1 | a) | | Discuss the key features of System Verilog and compare system Verilog with Verilog. | *CO-2* | *PO-1* | **8** |
| | b) | | Discuss the different types of code coverage with suitable examples. | *CO-1* | *PO--* | **12** |
| | | | **UNIT – II** | | | |
| 2 | a) | | Develop the Verilog RTL for a D Flip flop with asynchronous active high reset and synchronous set and test it by developing the System Verilog Test Bench using interface with clocking block and mod-ports. | *CO-4* | *PO-3* | **12** |
| | b) | | Discuss System Verilog event queue in detail. | *CO-1* | *PO--* | **8** |
| | | | **UNIT - III** | | | |
| 3 | a) | | Discuss the following:<br>i) Super ii) subclass iii) overriding iv) polymorphism v) automatic variable | *CO-1* | *PO--* | **10** |
| | b) | | What is the importance of constrained randomization? Discuss with an example. | *CO-2* | *PO-1* | **10** |
| | | | **OR** | | | |
| 4 | a) | | Develop a system Verilog RTL for a 4-bit adder with asynchronous reset pin. The adder is synchronized with a clock signal. | *CO-4* | *PO-3* | **8** |

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|---|---|---|---|---|---|---|
| | | b) | Develop a SV environment to i) randomize inputs for the design in 4a) using transactor class and ii) drive the inputs to the design using virtual interface | ***CO-4*** | ***PO-3*** | **12** |
| | | | **UNIT – IV** | | | |
| | 5 | a) | Discuss the following:<br>i)Concurrent assertions ii) property iii)sequence iv)assert_property | ***CO-1*** | ***PO--*** | **12** |
| | | b) | Using Concurrent Assertions, test for the following scenario:<br>→At posedge of clock<br>→check whether signal a is high<br>→if a is high, check whether signal b goes high after 1 clock cycle delay<br>→if true, then assert property | ***CO-2*** | ***PO-1*** | **8** |
| | | | **UNIT – V** | | | |
| | 6 | a) | Develop a Verilog RTL for a 4-bit Shift register with mode control for right and left shift operations. Also a load pin is asserted for parallel loading. | ***CO-4*** | ***PO-3*** | **8** |
| | | b) | Test the RTL in 6.a) by developing the following<br>i) Driver Class for defining functional covergroups and coverpoints, Randomizing, driving and sampling the coverage .<br>ii) Transactor class to define the constraints<br>iii) Program block, Interface and Top module | ***CO-4*** | ***PO-3*** | **12** |
| | | | **OR** | | | |
| | 7 | a) | Discuss the following with examples:<br>i) Covergroups and coverpoints<br>ii) Implicit and explicit bins | ***CO-1*** | ***PO--*** | **8** |
| | | b) | With a neat diagram, discuss the System Verilog layered test bench architecture. | ***CO-1*** | ***PO--*** | **12** |



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