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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**

Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

Course Code: 23EC6PE2SV / 22EC6PE2SV **Max Marks: 100**

Course: System Verilog and Verification

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)		Discuss Block coverage, Conditional coverage and Toggle coverage with a suitable example.	*1*	-	**8**
	b)		Design a divide by 8 synchronous up down counter and test the design using interface block and modports.	*4*	*3*	**12**
			OR			
2	a)		Design a T-FF with asynchronous active high reset and synchronous active low set. Write a test bench with interface block and modports to test the design.	*4*	*3*	**12**
	b)		Compare black box and white box verification.	*1*	-	**8**
			UNIT - II			
3	a)		Discuss system Verilog Event scheduling with neat illustrations.	*1*	-	**6**
	b)		Compare Dynamic arrays and associative arrays with examples.	*2*	*1*	**6**
	c)		Compare the different types of fork-join constructs in system Verilog with examples.	*2*	*1*	**8**
			OR			
4	a)		Compare Program Block and Module. Justify how the use of program block provides race free interaction between design and test bench.	*2*	*1*	**8**
	b)		Compare packed and unpacked arrays with suitable examples.	*2*	*1*	**6**
	c)		Discuss any two 2-state and 4-state data types in system Verilog with an example.	*1*	-	**6**

			UNIT - III			
	5	a)	Discuss the application of Inheritance in test bench environment with suitable examples.	*2*	*1*	**8**
		b)	Design an RTL to add or subtract 2 four-bit numbers based on control signal. Develop a SV randomized test bench using Driver Class with Virtual interface to drive the inputs to the design at posedge of clock.	*4*	*3*	**12**
			OR			
	6	a)	Discuss the need for Randomization in the test bench. Also Discuss the use of constrained randomization with suitable examples.	*2*	*1*	**8**
		b)	Design an RTL for a 4-bit up/down counter based on a control signal. Develop a SV test bench using Driver Class to drive the inputs to the design at posedge of clock using Virtual interface.	*4*	*3*	**12**
			UNIT - IV			
	7	a)	Distinguish between immediate assertions and concurrent assertions with suitable examples.	*2*	*1*	**10**
		b)	Discuss Sequence repetition operators with examples.	*1*	-	**10**
			OR			
	8	a)	Discuss sequence and property in concurrent assertions.	*1*	-	**10**
		b)	For a divide by 8 counter, develop a SVA based test bench to check for following assertions: i) When Counter value reaches 7 ii) When Counter is reset	*2*	*1*	**10**
			UNIT - V			
	9	a)	What is a mailbox? Discuss some of the methods used for creating, putting and retrieving messages from mailbox.	*1*	-	**10**
		b)	Discuss functional coverage using covergroups and coverpoints with a suitable example.	*1*	-	**10**
			OR			
	10	a)	With a neat diagram, discuss the System Verilog layered test bench architecture.	*1*	-	**10**
		b)	Discuss the different coverage options which create the bins for each coverpoint variable defined inside a covergroup.	*1*	-	**10**

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