U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

July 2023 Semester End Main Examinations

Programme: B.E. **Semester: VI**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC6PE3SV **Max Marks: 100**
Course: System Verilog and Verification **Date: 17.07.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Discuss the different types of code coverage with suitable examples.	*CO2*	*PO 1*	**12**
	b)		Discuss some key features of system Verilog and compare system Verilog with Verilog.	*CO 2*	*PO 1*	**08**
			UNIT - II			
2	a)		Develop the Verilog RTL for a JK Flip flop with asynchronous active high reset and synchronous set inputs. Test this by developing the System Verilog Test Bench using interface with clocking block and modports.	*CO 3*	*PO 2*	**12**
	b)		Discuss Dynamic arrays and associative arrays with examples.	*CO 2*	*PO 1*	**08**
			UNIT - III			
3	a)		What is inheritance? Discuss its application with suitable examples.	*CO 2*	*PO 1*	**06**
	b)		Develop an RTL to add or subtract 2 four-bit numbers based on control signal. Develop a randomized test bench using transactor and driver to drive the random numbers to the design at posedge of clock.	*CO 3*	*PO 2*	**14**
			OR			
4	a)		What is Randomization? Discuss constrained randomization with suitable examples.	*CO 2*	*PO 1*	**10**
	b)		Explain virtual interface with an example. What is Polymorphism?	*CO 2*	*PO 1*	**10**
			UNIT - IV			
5	a)		Distinguish between immediate assertions and concurrent assertions with suitable examples.	*CO 2*	*PO 1*	**10**
	b)		Discuss in detail sequence and property.	*CO 1*	--	**10**

			UNIT - V			
	6	a)	Develop a Mealy FSM that detects "0100" sequence with overlap.	*CO 3*	*PO 2*	**08**
		b)	Test the RTL in 6.a) by developing the following i) Driver Class for defining functional covergroups and coverpoints, Randomizing, driving and sampling the coverage . ii) Transactor class to define the constraints iii) Program block, Interface and Top module	*CO 3*	*PO 2*	**12**
			OR			
	7	a)	With a neat diagram, discuss the System Verilog layered test bench architecture.	*CO 1*	--	**10**
		b)	What are the different coverage options which create the bins for each coverpoint variable defined inside a covergroup?	*CO 1*	--	**10**

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