U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**

Branch: Electronics & Communication **Duration: 3 hrs.**

Course Code: 19EC6PE3SV **Max Marks: 100**

Course: System Verilog and Verification

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	***CO***	***PO***	**Marks**
1	a)		List some of the key features of System Verilog and compare system Verilog with Verilog.	*1*	-	**8**
	b)		Discuss the different types of code coverage with suitable examples.	*1*	-	**12**
			OR			
2	a)		Discuss the importance of Verification in a typical ASIC Flow. Describe how the Direct Testing is different from Random Testing.	*1*	-	**12**
	b)		Describe the different functional verification approaches.	*1*	-	**8**
			UNIT - II			
3	a)		Develop the Verilog RTL for a JK Flip flop with asynchronous active high reset and synchronous set and test it by developing the System Verilog Test Bench using interface with clocking block and modports.	*4*	*3*	**12**
	b)		Analyze System Verilog event scheduling in detail.	*2*	*1*	**8**
			OR			
4	a)		Develop the Verilog RTL for a Mod 16 counter and test it by writing the System Verilog Test Bench Environment using interface with clocking block and modport constructs.	*4*	*3*	**12**
	b)		Distinguish between Program block and module.	*2*	*1*	**8**
			UNIT - III			
5	a)		Briefly discuss the following terms with an example for each i. Inheritance ii. super	*1*	-	**10**

		b)	Discuss the various fork-join constructs in System Verilog with suitable examples.	*1*	-	**10**
			OR			
	6	a)	Discuss the following: i) Overriding ii) Polymorphism	*1*	-	**10**
		b)	What is constrained randomization? How is it useful in Verification? Discuss with an example.	*1*	-	**10**
			UNIT - IV			
	7	a)	Using assertions develop the System Verilog Assertion based Randomized Testbench and RTL for 4-bit synchronous counter and generate the assertions only when the output count value is 5.	*2*	*1*	**10**
		b)	Discuss the following with an example: i) Sequence ii) Property iii) assert property	*1*	-	**10**
			OR			
	8	a)	Distinguish between immediate and concurrent assertions.	*1*	-	**10**
		b)	Using Concurrent Assertions, test for the following scenario: →At posedge of clock →check whether signal a is high →if a is high, check whether signal b goes high after 1 clock cycle delay →if true, then assert property	*2*	*1*	**10**
			UNIT - V			
	9	a)	Discuss in detail the System Verilog Layered Testbench Architecture.	*1*	-	**10**
		b)	What are the different coverage options which create the bins for each coverpoint variable defined inside a covergroup?	*1*	-	**10**
			OR			
	10	a)	Discuss the following with examples: i) Covergroups and coverpoints ii) Implicit and explicit bins	*1*	-	**10**
		b)	Discuss Illegal bins and Ignore bins with suitable examples.	*1*	-	**10**

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