U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**

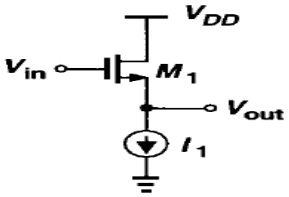
Branch: Electronics & Communication Engineering **Duration: 3 hrs.**

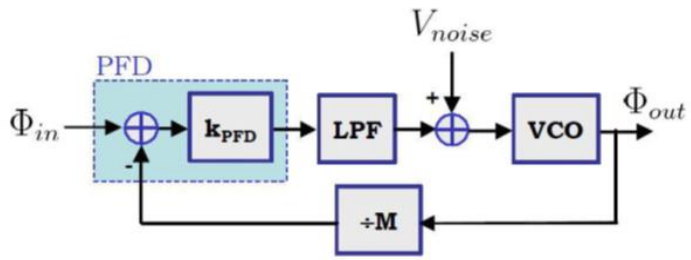
Course Code:16EC6DCMSD **Max Marks: 100**

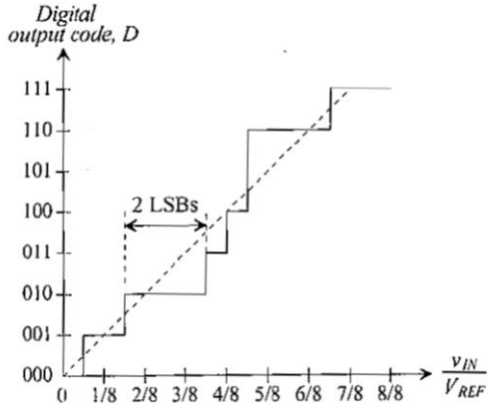
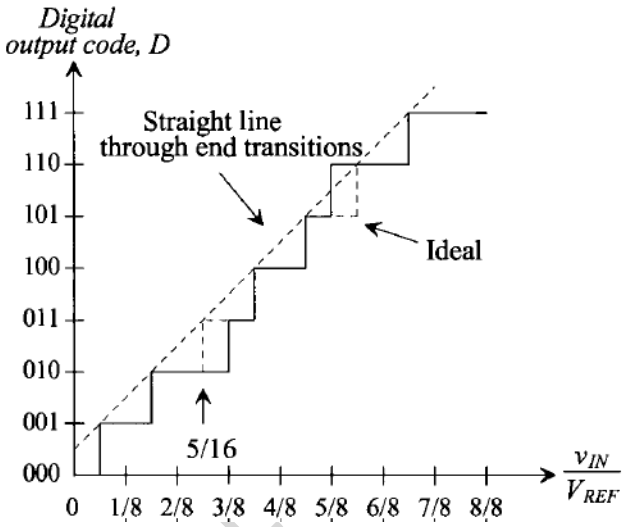
Course: Mixed Signal Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)		Analyze the given circuit to obtain Vout if $(W/L)_1 = 20/0.5$. $I_D = 200\mu A$, $V_{th} = 0.6V$, $\mu_n C_{ox} = 50\ \mu A/V^2$,$V_{in} = 1.2V$  Fig1	*2*	*2*	**10**
	b)		Illustrate the working of common source amplifier with Resistive load	*1*	*1*	**10**
			OR			
2	a)		Deduce the representation of the minimum and maximum differential input voltage as well as common mode input voltage swing for a source-coupled Differential amplifier.	*1*	*1*	**10**
	b)		Perform the qualitative analysis of a differential pair circuit with the help of input output characteristics plots. Illustrate that small-signal gain is maximum for equal inputs.	*2*	*2*	**10**
			UNIT - II			
3	a)		Implement a two stage opamp with single ended output and obtain the overall voltage gain starting with the simple two stage opamp	*1*	*1*	**10**
	b)		Describe op amp design parameters also mention its importance.	*1*	*1*	**10**

			OR			
	4	a)	Highlight the drawbacks of a single stage Opamp and Show the implementation which can overcome the same.	*1*	*1*	**10**
		b)	Implement a two stage opamp with single ended output and obtain the overall voltage gain starting with the simple two stage opamp	*1*	*1*	**10**
			UNIT - III			
	5	a)	Analyze the linear model of type 1 PLL assuming under damped system and also obtain the expression for $\omega_{out}(t)$, when the input is a frequency step.	*2*	*2*	**10**
		b)	Describe the various performance parameters of a VCO.	*1*	*1*	**10**
			OR			
	6	a)	A VCO senses a sinusoidal control voltage Vcont = Vm cos ωmt, determine the output waveform and spectrum, justify your answer with appropriate description.	*2*	*2*	**10**
		b)	A linear model of a PLL with an active loop filter is shown in figure 2. Derive an expression for the transfer function of the VCO (i.e. φout/vout, where vout and φout are the control voltage and the output phase of the VCO, respectively).  Figure-2	*1*	*1*	**10**
			UNIT - IV			
	7	a)	In a 3 bit R-2R DAC if R=1.1KΩ and 2R= Rf =2KΩ, determine the maximum INL and DNL for the converter. (Assume ideal case to be R=1KΩ). Assume all the switches to be ideal and V_{REF}=5V.	*2*	*2*	**10**
		b)	Justify the need to address the Mixed Signal issues in chip design	*1*	*1*	**10**
			OR			
	8	a)	Identify different errors in Figure-3. Calculate DNL for each digital code and maximum resolution of the converter.	*1*	*1*	**10**

			 Figure-3			
		b)	Determine the INL for the 3 bit ADC whose transfer curve is shown in Fig-4 Assume that V_{Ref} = 5 V. Draw the quantization error, Qe, in units of LSBs.  Fig-4	*1*	*1*	**10**
			UNIT - V			
	9	a)	Design a 3-bit DAC using an R-2R architecture with R = 1 kΩ, R_F= 2kΩ, and V_{REF}= 5V. Assume that the resistances of the switches are negligible. Determine the value of I_{T0T} for each digital input and the corresponding output voltage, $V_{0UT.}$Represent the same on a circuit and tabulate the output voltages.	*3*	*3*	**10**
		b)	Illustrate the working of a pipeline ADC. What are the advantages and drawbacks of the same?	*1*	*1*	**10**
			OR			
	10	a)	Design a 3-bit charge-scaling DAC and find the value of the output voltage for $D_2D_1D_0$= 010 and 101. Assume that V_{ref}= 5 V and C= 0.5 pF.	*3*	*3*	**10**
		b)	Illustrate the binary search operation in a Successive Approximation ADC with a suitable example.	*1*	*1*	**10**

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