U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

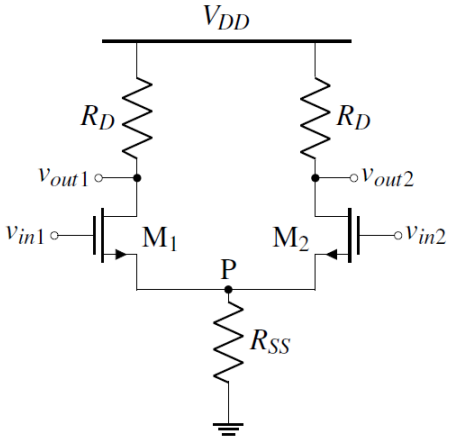
Autonomous Institute Affiliated to VTU

July 2023 Semester End Main Examinations

Programme: B.E. **Semester: VI**
Branch: Electronics and Communications Engineering **Duration: 3 hrs.**
Course Code: 16EC6DCMSD **Max Marks: 100**
Course: Mixed Signal Design **Date: 10.07.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Obtain the small-signal voltage gain of a source follower and also analyze the nonlinearity and the voltage headroom limitation.	*CO2*	*PO2*	**10**
	b)	A differential amplifier shown in Figure 1 uses resistor than current source to define tail current of 1 mA. Assume $(W/L)_{1,2} = 20/0.5$, $\mu_n C_{ox} = 60\ \mu A/V2$, $V_{TH} = 0.6$ V, $\lambda = \gamma = 0$ and $V_{DD} = 3$ V. (i) What is the required input CM for which R_{SS} sustains 0.5 V? (ii) Calculate R_D for a differential gain of 5. What happens at the output if the input CM level is 30 mV higher than the value calculated in (a)?  Fig. 1: Question 1.(b)	*CO1*	*PO1*	**10**
		UNIT – II			
2	a)	Justify the importance of op-amp design parameters from the point of view of system design.	*CO1*	*PO1*	**10**
	b)	Justify how two stage op-amps can overcome the gain and output swing limitation encountered by cascode op-amp.	*CO*	*PO*	**10**

			UNIT - III			
	3	a)	A VCO senses a small sinusoidal control voltage $V_{cont} = V_m \cos(\omega_m t)$. Determine the output waveform and its spectrum.	*CO1*	*PO1*	**10**
		b)	Calculate the change in phase error if type 1 PLL experiences a frequency step $\Delta\omega$ at $t = 0$.	*CO1*	*PO1*	**06**
		c)	Demonstrate the implementation of a simple PLL in CMOS technology with necessary explanation.	*CO1*	*PO1*	**04**
			OR			
	4	a)	Obtain the transfer function of charge-pump PLL. Discuss the stability issues.	*CO1*	*PO1*	**10**
		b)	Illustrate the relevance of various performance parameters of a VCO in the context of PLL design.	*CO1*	*PO1*	**10**
			UNIT - IV			
	5	a)	A S/H circuit settles to within 1 percent of its final value at 6 µs. What is the maximum resolution and speed with which an ADC can use this data assuming that the ADC is ideal?	*CO1*	*PO1*	**06**
		b)	Determine the maximum DNL (in LSBs) for a 3-bit DAC, which has the following characteristics. Does the DAC have 3-bit accuracy? If not, what is the resolution of the DAC having this characteristic?	*CO1*	*PO1*	**06**
		c)	Establish the relevance of any four specifications of DAC.	*CO1*	*PO1*	**08**
			UNIT - V			
	6	a)	For the cyclic DAC, determine the gain error for a 3-bit conversion if the feedback amplifier had a gain of 0.45V/V. Assume that V_{ref}=5V.	*CO1*	*PO1*	**06**

Digital Input	Voltage Output (V)
000	0
001	0.625
010	1.5625
011	2.0
100	2.5
101	3.125
110	3.4375
111	4.275

		b)	Identify the disadvantages of single slope integrating ADC and explain the circuits used to overcome these disadvantages.	*CO1*	*PO1*	**10**
		c)	Design a 3-bit generic current-steering DAC. Assume that each current source I is 10 μA. Find the total output current for each input code.	*CO3*	*PO3*	**04**
			OR			
	7	a)	Illustrate the working of a cyclic ADC with a suitable example.	*CO1*	*PO1*	**10**
		b)	Explain the principle of successive approximation. Assume that Vin = 2.6 V, V_{REF} = 5 V and 4-bit for the successive approximation ADC and that the comparator, because of its offset, makes the wrong decision for the MSB conversion. What will be the final digital output?	*CO1*	*PO1*	**10**

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