U.S.N.										

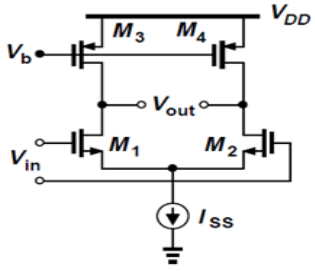
B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

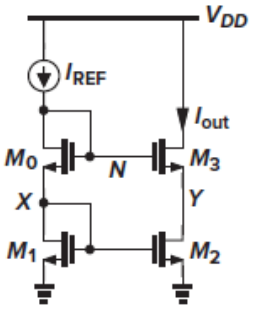
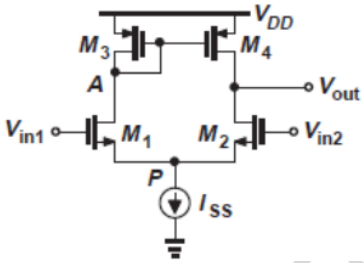
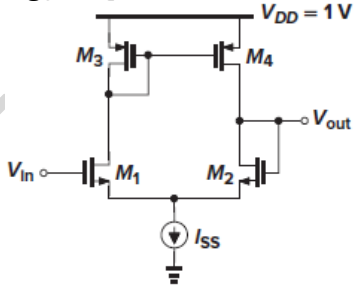
July 2023 Semester End Main Examinations

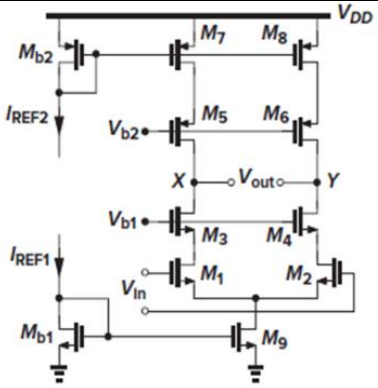
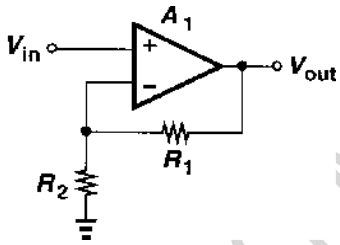
Programme: B.E. **Semester: VI**
Branch: Electronics and Communications Engineering **Duration: 3 hrs.**
Course Code: 19EC6PCMSD **Max Marks: 100**
Course: Mixed Signal Design **Date: 10.07.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			UNIT - I	***CO***	***PO***	**Marks**
	1	a)	An NMOS device carries 1 mA with $V_{GS} - V_{th} = 0.6V$ and 1.6 mA with $V_{GS} - V_{th} = 0.8V$, both with the same V_{DS}. If the device operates in the triode region, calculate V_{DS} and W/L. Assume $\mu_n C_{ox} = 200\ \mu A / V^2$ and $V_{th} = 0.4V$	*CO1*	*PO1*	**06**
		b)	Analyse a source follower with resistive load and obtain an expression for the small-signal voltage gain.	*CO2*	*PO2*	**06**
		c)	Analyse a cascode amplifier and obtain the input – output characteristics.	*CO2*	*PO2*	**08**
			UNIT - II			
	2	a)	Obtain the expression for the common mode gain of a differential amplifier assuming circuit is symmetric but current source has finite output impedance. What inference can be drawn from this?	*CO1*	*PO1*	**07**
		b)	Calculate the differential voltage gain if I_{SS} = 1 mA, $(W/L)_{1,2}$ = 50/0.5, and $(W/L)_{3,4}$ = 50/1. Given λ_n = 0.1/V, λ_p = 0.2/V, V_{THn} = 0.7V, V_{THp} = - 0.8V, $\mu_n C_{ox}$ = 135 $\mu A/V^2$ and $\mu_p C_{ox}$ = 35$\mu A/V^2$. What is the minimum allowable input CM level if I_{SS} requires at least 0.4 V across it? 	*CO1*	*PO1*	**07**
		c)	In the figure shown, if I_{ref} requires 0.5V to operate as a current source, what is its maximum value? Determine this value if V_{DD} = 3V, V_{th} = 0.6V, $\mu_n C_{ox}$ = 50 $\mu A/V^2$ and W/L = 25/0.5 for all transistors.	*CO1*	*PO1*	**06**

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

						
			UNIT - III			
	3	a)	Design the circuit for a voltage gain of 30 and I_{SS} = 1.1mA with V_{DD} = 1.8 V. Assume M_1 operates at the edge of saturation if the input common-mode level is 1 V. Also, $\mu_n C_{ox} = 2\mu_p C_{ox} = 100\ \mu A/V^2$, $V_{TH,n} = 0.5V$, $V_{TH,p} = -0.4V$, $\lambda_n = 0.5\lambda_p = 0.1/V$. 	*CO3*	*PO3*	**09**
		b)	Demonstrate the circuit of a 2-stage op-amp with a fully differential Telescopic Op-Amp as the first stage. Write the expressions for their overall voltage gains. Identify the drawback of the telescopic op-amp with appropriate justification.	*CO1*	*PO1*	**07**
		c)	Determine the input common-mode voltage range of the unity-gain buffer given that each device, including the current source has a threshold voltage of 0.3V and an overdrive voltage of 0.1V. 	*CO1*	*PO1*	**04**
			OR			
	4	a)	Determine the aspect ratio of transistors $M_1 - M_9$ in the circuit shown, for the following specifications: V_{DD} = 3 V, peak – to – peak differential output swing = 3 V, power dissipation = 10 mW, voltage gain = 2000. Assume $\mu_n Cox$ = 60 $\mu A/V^2$, $\mu_p Cox$ = 30 $\mu A/V^2$, λn = 0.1 V^{-1}, λp = 0.1 V^{-1} (for an effective channel length of 0.5 μm), $\gamma = 0$, Vthn = |Vthp| = 0.7 V.	*CO1*	*PO1*	**10**

						
	b)	For a differential amplifier with current mirror load, perform large signal analysis and draw its input-output characteristic.	*CO2*	*PO2*	**07**
	c)	The circuit shown is designed for a nominal gain of 10, i.e., $1 + R_1/R_2 = 10$. Determine the minimum value of A_1 for a gain error of less than 1%. 	*CO1*	*PO1*	**03**
		UNIT - IV			
5	a)	Realize a non-inverting amplifier using switched capacitors and explain its working.	*CO3*	*PO3*	**07**
	b)	Demonstrate the construction of an integrator using switched capacitor circuits. Draw its output waveform and write the output equation.	*CO1*	*PO1*	**06**
	c)	Design a precision multiply – by – 2 circuit using switched capacitors.	*CO3*	*PO3*	**07**
		UNIT - V			
6	a)	Define DNL with reference to a DAC. What should be the minimum value of DNL to exhibit monotonicity? Determine the value of 1 LSB, percentage accuracy and full-scale voltage of 3-bit, 6-bit and 8-bit DAC assuming $V_{REF} = 5V$.	*CO1*	*PO1*	**06**
	b)	Determine the conversion time of a single slope integrating ADC. Briefly describe its working with the help of block diagram.	*CO1*	*PO1*	**07**
	c)	Design a 3-bit generic current-steering DAC with each current source I = 5 μA. Find the total output current for each input code. What is its advantage over R – 2R DAC?	*CO3*	*PO3*	**07**
		OR			

	7	a)	Establish the relevance of the following terms with reference to ADC (i) Quantization error (ii) Aliasing (iii) Offset error (iv) INL	*CO1*	*PO1*	**04**
		b)	Design a 3-bit charge-scaling DAC and find the value of the output voltage for $D_2D_1D_0$ = 010 and 110. Assume that V_{REF} = 5 V and C= 0.5 pF. Write the equation for the output voltage.	*CO3*	*PO3*	**05**
		c)	Demonstrate the implementation of binary search principle in the successive approximation ADC. Determine the final output of the ADC if V_{in} = 3V, V_{REF} = 5V and an 8-bit DAC is used.	*CO1*	*PO1*	**11**

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