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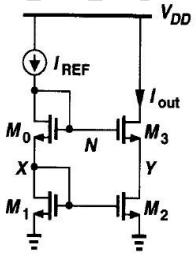
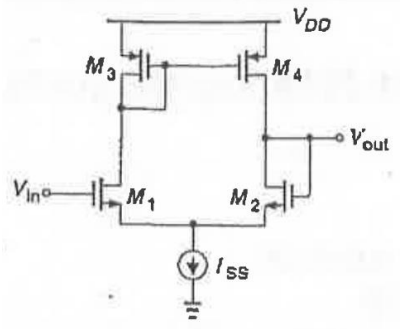
B.M.S. College of Engineering, Bengaluru-560019

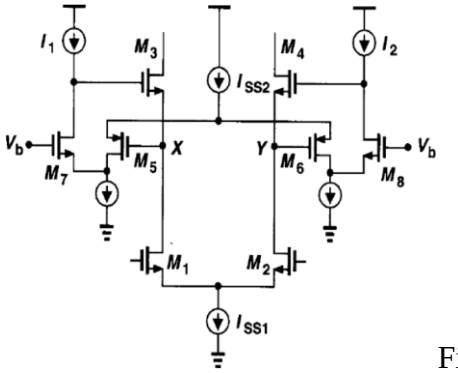
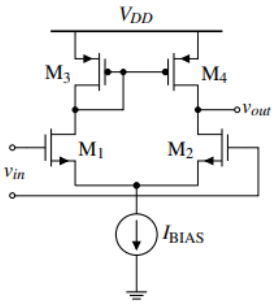
Autonomous Institute Affiliated to VTU

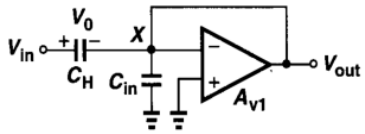
September / October 2024 Supplementary Examinations

Programme: B.E. **Semester: VI**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC6PCMSD **Max Marks: 100**
Course: Mixed Signal Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			UNIT - I	CO	PO	Marks
1	a)		A source follower using NMOS current source, which operates as a level shifter is designed to increase the output level by 1V than the input level.Determine the sizes of the transistors if $I_{D1}=I_{D2}=0.5mA$, $V_{GS2}-V_{GS1}=0.5V$, $\mu_n C_{ox}=100\mu A/V^2$, $V_{TH}=0.7V$, $\lambda=\gamma=0$.	CO1	PO1	**8**
	b)		Illustrate the working of common source amplifier with resistive load.	CO1	PO1	**6**
	c)		For the circuit shown in Fig. 1, if I_{REF} requires 0.5 V to operate as a current source, Determine its maximum value?  Fig. 1	CO1	PO1	**6**
			UNIT - II			
2	a)		Determine the input common-mode voltage range and the closed loop output impedance of the unity gain buffer shown below in Fig. 2, given: threshold voltage of each device 0.7 V and overdrive voltage 0.3 V. Comment on the result**.**  Fig. 2	CO1	PO1	**10**

		b)	Identify the type of amplifier in Fig. 3, employed in boosting the gain. Also determine the output impedance at the drain of transistor M_3. (Replace ideal current sources with transistors for the calculation). Assume g_{mn} = 1 mA/V, g_{mp} = 2 mA/V and r_{on} = 5 k, r_{op} = 10 k.  Fig. 3	*CO2*	*PO2*	**5**
		c)	Discuss about input range limitations of unity-gain buffer.	*CO1*	*PO1*	**5**
			UNIT - III			
	3	a)	Perform the large signal analysis of a differential pair with current mirror load. Also work out the limits on input and output voltage swings.	*CO2*	*PO2*	**10**
		b)	Consider the differential amplifier circuit of Figure 4, I_{Bias} = 200 µA and all transistors have W/L =(100 µm/1.6 µm). Given that $\mu_n C_{ox}$ = 92 µA/V^2 , Vth = 0.8 V, and r_{ds} = 8000×L(µm)/I_D(mA). Determine the gain from the differential input to the output.  Fig. 4	*CO1*	*PO1*	**10**
			OR			
	4	a)	List op-amp design parameters and also discuss their importance.	*CO1*	*PO1*	**10**
		b)	Design a folded cascade op-amp with a PMOS input pair to satisfy the following specifications: V_{DD} = 3 V, Maximum differential swing= 2.4 V, total power dissipation= 6 mW, minimum voltage gain= 200. Assume $\mu_n C_{ox}$ = 60 µA/V^2 , $\mu_p C_{ox}$ = 30 µA/V2 , λ_n = 0.1 V^{-1} , λ_p = 0.2 V^{-1} , γ = 0, V_{THn} = $\lvert V_{THp} \rvert$ = 0.7 V, V_{ISS} = 0.3 V and V_O for input pair is 0.53V.	*CO3*	*PO3*	**10**
			UNIT - IV			
	5	a)	With the help of a neat circuit diagram, discuss the operation of a fully differential amplifier built using switched capacitors.	*CO1*	*PO1*	**8**
		b)	Design a non-inverting amplifier using switched capacitors.	*CO3*	*PO3*	**6**

		c)	In the circuit shown in Figure 5, C_{in} = 0.5 pF and C_H = 2 pF. Determine the minimum op amp gain that guarantees a maximum gain error of 0.1%?  Fig. 5	*CO1*	*PO1*	**6**
			UNIT - V			
	6	a)	Discuss mixed signal layout issues at system, device and interconnect levels.	*CO1*	*PO1*	**10**
		b)	Plot the transfer curve of a 3-bit R-2R DAC if R = 1.1 kΩ and 2R = 2 kΩ by making a table of the actual output voltage for each input combinations. Label the node voltage for each input combination, given V_{REF} = 5 V. If the switches are ideal, determine the maximum INL and DNL of the converter.	*CO2*	*PO2*	**10**
			OR			
	7	a)	With the help of neat diagram discuss the construction and working of charge-scaling DACs.	*CO1*	*PO1*	**10**
		b)	Compare the various types of ADC and also discuss the principles of successive approximation ADC.	*CO2*	*PO2*	**10**

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