U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**

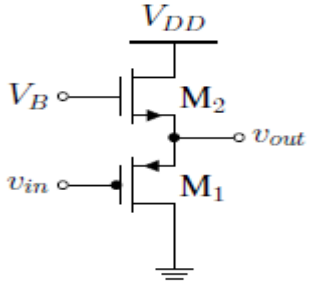
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

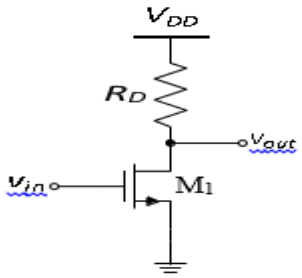
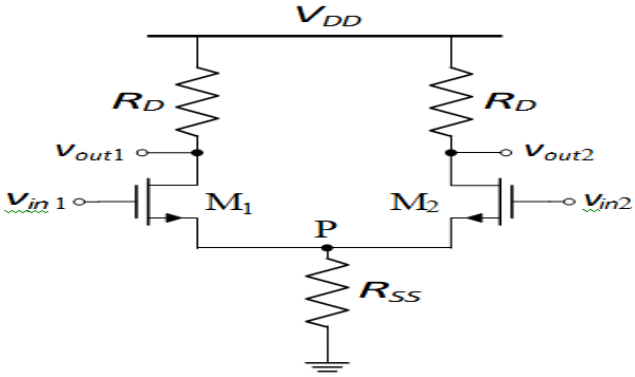
Course Code: 19EC6PCMSD **Max Marks: 100**

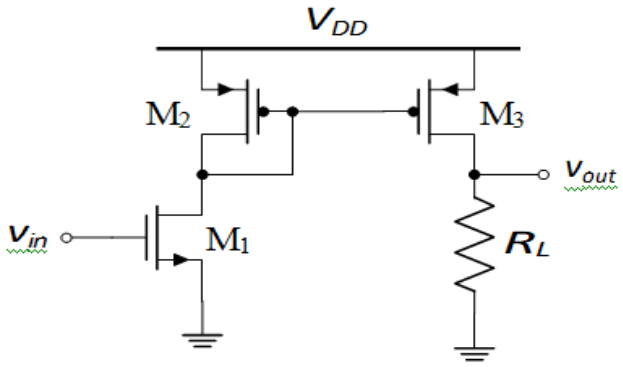
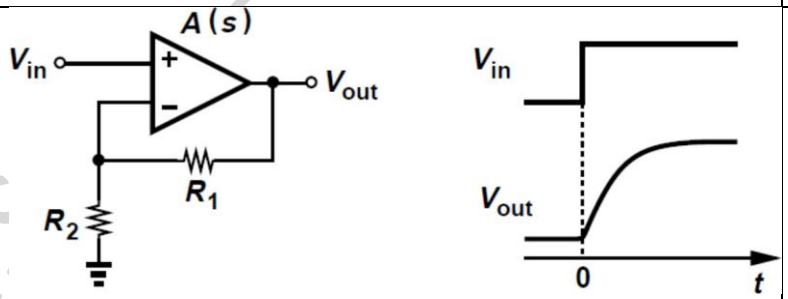
Course: MIXED SIGNAL DESIGN

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Obtain the small-signal voltage gain of a common source stage with resistive load with channel length modulation taken into account. Also draw the small-signal equivalent model.	CO1	PO 1	10
	b)	A source follower using NMOS current source shown in Figure which operates as a level shifter is designed to increase the output level by 1 V than the input level. Calculate the sizes of both the transistors if $ID1 = ID2 = 0.5$ mA; $VGS2 - VGS1 = 0.5$ V, $\mu nCox = 100\ \mu$A/V2, $VTH = 0.7$ V, $\lambda = \gamma = 0$. 	CO1	PO1	10
		OR			
2	a)	For the circuit shown in the Figure, if $(W/L) = 50/0.5$, $R_D = 2$ kΩ, $\lambda = 0$ and $\mu_n C_{ox} = 1.34225 \times 10^{-4}$ A/V^2, $V_{th} = 0.7$ V, $V_{DD} = 3$ V. (a) What is the small signal gain if M_1 is in saturation and $I_D = 1$ mA? (b) What input voltage places M_1 at the edge of triode region? What is the small-signal gain under this condition?	CO1	PO1	10

						
		b)	Demonstrate that the Common-Source Common-Gate cascode amplifier has: (i)Superior gain compared to a common-source amplifier for same voltage swing (ii) smaller difference in drain currents due to a difference in drain voltages than without the stacking transistor (shielding property)	*CO1*	*PO1*	**10**
			UNIT - II			
	3	a)	Perform the qualitative analysis of a differential pair circuit with the aid of input output characteristics plots. Illustrate that small-signal gain is maximum for equal inputs.	*CO1*	*PO1*	**10**
		b)	A differential amplifier shown in Figure uses resistor than current source to define tail current of 1 mA. Assume $(W/L)_{1,2}$ = 25/0.5, µnCox = 50 µA/V2, V_{TH} = 0.6 V, λ = γ = 0 and V_{DD} = 3 V. (a)What is the required input CM for which R_{SS} sustains 0.5 V? (b)Calculate R_D for a differential gain of 5. (c)What happens at the output if the input CM level is 50 mV higher than the value calculated in (a)? 	*CO2*	*PO2*	**10**
			OR			
	4	a)	Justify the need for current mirrors in integrated circuit design. Consider the circuit in the Figure with R_L = 10 kΩ, V_{DD} = 1.8 V and NMOS (M1): I_{D1} = 100 µA, $(W/L)_1$ = 50 µm/1 µm, µnCox = 120 µA/V2. PMOS (M2): $(W/L)_2$ = 100 µm/1 µm, µpCox = 60 µA/V2. PMOS (M3): $(W/L)_3$ = 100 µm/1 µm, µpCox = 60 µA/V2. Neglecting channel length modulation, determine (i) the output DC (or average) voltage	*CO1*	*PO1*	**10**

			(ii) the small-signal voltage gain 			
		b)	Perform the quantitative analysis of a differential pair circuit and calculate the differential output current. Indicate the variations of drain currents and the overall trans-conductance of differential pair versus input voltage.	*CO1*	*PO1*	**10**
			UNIT - III			
	5	a)	Design a telescopic cascode op-amp to satisfy the following specifications: V_{DD}=3V, differential output swing = 3 V, power dissipation = 10 mW, voltage gain = 1000. Assume $\mu nCox$=60 μAV2⁄, $\mu pCox$=30 μAV2⁄, λn=0.1 V^{-1}, λp=0.2 V^{-1}, γ=0, V_{TN}=$\lvert V_{TP}\rvert$=0.7 V.	*CO3*	*PO3*	**10**
		b)	With the help of neat circuit diagram and appropriate analyses, obtain the small-signal gain of a differential pair with current mirror load in differential and common-mode.	*CO2*	*PO2*	**10**
			OR			
	6	a)	 In the circuit of Figure assume the Op-Amp is a single pole voltage amplifier. If Vin is a small step, calculate the time required for the output voltage to reach within 1% of its final value. What unity-gain bandwidth must the Op-Amp provide if 1 + R1/R2 ≈ 10 and the settling time is to be less than 5 ns? For simplicity, assume that the low-frequency gain is much greater than unity.	*CO1*	*PO1*	**10**
		b)	It is required to boost the output impedance of a differential cascade stage. Suggest a suitable circuit and illustrate how output impedance can be boosted substantially with appropriate descrip-tion.	*CO1*	*PO1*	**10**

			UNIT - IV			
	7	a)	Realize a non-inverting amplifier using switched capacitors and explain its working.	*CO3*	*PO3*	**7**
		b)	Demonstrate the construction of an integrator using switched capacitor circuits. Draw its output waveform and write the output equation.	*CO1*	*PO1*	**6**
		c)	Briefly discuss any two phenomena that affect the precision of sampled analog voltages.	*CO1*	*PO1*	**7**
			OR			
	8	a)	With the help of neat circuit diagrams, demonstrate the operation of a multiply-by-two circuit in sampling mode and amplification mode.	*CO1*	*PO1*	**7**
		b)	What is the need for common-mode feedback in fully differential amplifiers? Demonstrate how switched capacitors can be employed for it.	*CO1*	*PO1*	**8**
		c)	Discuss the limitations of using a single NMOS and PMOS transistor as a sampling switch and how a transmission gate improves the performance.	*CO1*	*PO1*	**5**
			UNIT - V			
	9	a)	Explain the principle of successive approximation. Assume that V_{in} = 2.49 V, V_{REF} = 5 V and 4-bit for the successive approximation ADC and that the comparator, because of its offset, makes the wrong decision for the MSB conversion. What will be the final digital output?	*CO3*	*PO3*	**10**
		b)	Discuss mixed signal layout issues.	*CO1*	*PO1*	**10**
			OR			
	10	a)	Design a 3-bit charge-scaling DAC and find the value of the output voltage for $D_2D_1D_0$ = 010 and 110. Assume that V_{REF} = 5 V and C= 0.5 pF. Write the equation for the output voltage.	*CO3*	*PO3*	**8**
		b)	Establish the relevance of the following terms with reference to ADC (i) Quantization error (ii) Aliasing (iii) Offset error (iv) INL	*CO1*	*PO1*	**4**
		c)	Explain the working of a single slope integrating ADC with the help of block diagram and discuss the accuracy issues related to the same.	*CO1*	*PO1*	**8**

****