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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: VI**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC6PCMSD **Max Marks: 100**
Course: Mixed Signal Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) For the circuit shown in Figure 1, given (W/L) = 50/0.5, $\mu_n C_{ox} = 135\ \mu\text{A/V}^2$, $\lambda = 0$, $R_D = 2$ kΩ, $V_T = 0.7$ V and $V_{DD} = 3$ V; what input voltage places M_1 at the edge of triode region? What is the output voltage under this condition? **08**

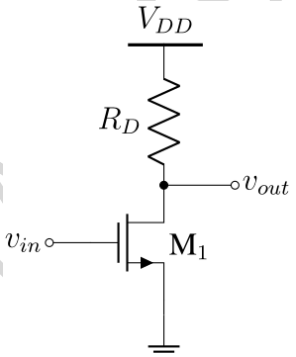

Figure 1: Question 1.(a)

b) With the help of neat diagrams, illustrate the operation of a source follower and mention its applications. **07**

c) Demonstrate that the Common-Source Common-Gate cascode amplifier has superior gain compared to a common-source amplifier for same voltage swing. **05**

UNIT - II

2 a) Perform the quantitative analysis of a differential pair circuit and calculate the differential output current. Also, indicate the dependence of the overall transconductance of the differential pair on the input voltage. **10**

b) A differential amplifier shown in Figure 2 uses a resistor to define the tail current of 1 mA with the given parameters: $(W/L)_{1,2}$ = 25/0.5, $\mu_n C_{ox} = 50\ \mu\text{A/V}^2$, $V_T = 0.6$ V and $V_{DD} = 3$ V. Calculate R_D for a differential gain of 10. **04**

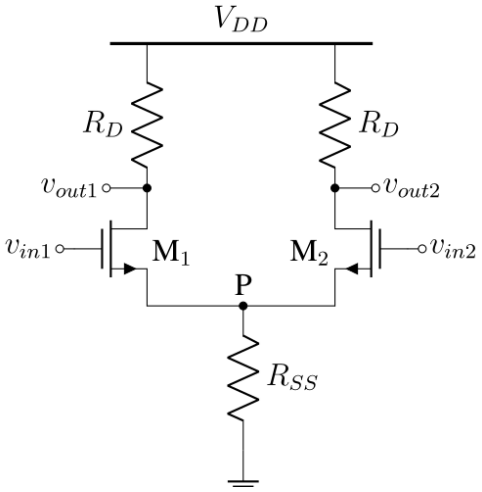

Figure 2: Question 2.(b)

c) What is the need for a cascode current mirror in an analog integrated circuit? Also show how the biasing can be obtained. **06**

UNIT - III

3 a) With the help of neat circuit diagram and appropriate analyses, obtain the small-signal differential gain of a differential pair with current mirror load. **10**

b) A single pole Op-Amp of DC gain 2000 and unity-gain bandwidth 10 Grad/s is used to realize a non-inverting amplifier of gain 5. For a step input, calculate the time needed for the output to reach within 2% of its final value. **06**

c) Highlight the drawback of a single-stage op-amp and show how the two-stage implementation which can overcome the same. **04**

OR

4 a) Design a telescopic cascode op-amp to satisfy the following specifications: $V_{DD} = 3$V, differential output swing = 3 V, power dissipation = 10 mW, voltage gain = 1000. Assume $\mu_n C_{ox} = 60\ \mu\text{A/V}^2$, $\mu_p C_{ox} = 30\ \mu\text{A/V}^2$, $\lambda_n = 0.1\ V^{-1}$, $\lambda_p = 0.2\ V^{-1}$, $\gamma = 0$, $V_{TN} = |V_{TP}| = 0.7$ V. **10**

b) The circuit shown in Figure 3 is designed for a nominal gain of 20. Determine the minimum value of A_1 for a gain error of 0.5%. **04**

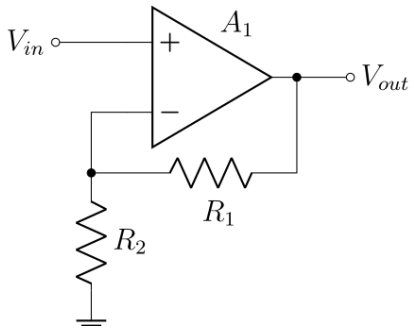

Figure 3: Question 4.(b)

c) With the help of a neat circuit diagram, briefly describe the technique of gain boosting. (Small-signal analysis not needed) **06**

UNIT - IV

5 a) Demonstrate that a switched-capacitor can lead to the realization of a large resistance on-chip. Also highlight the limitations of such a realization. **07**

b) What is the need for common-mode feedback in fully differential amplifiers? Demonstrate how switched capacitors can be employed for it. **08**

c) A unity-gain buffer in sampling mode is shown in Figure 4, where the input voltage V_0 is sampled onto the capacitor C_H. What is the minimum op amp gain A_1 that guarantees a maximum gain error of 0.1%, given C_{in} = 0.5 pF and C_H = 2 pF? **05**

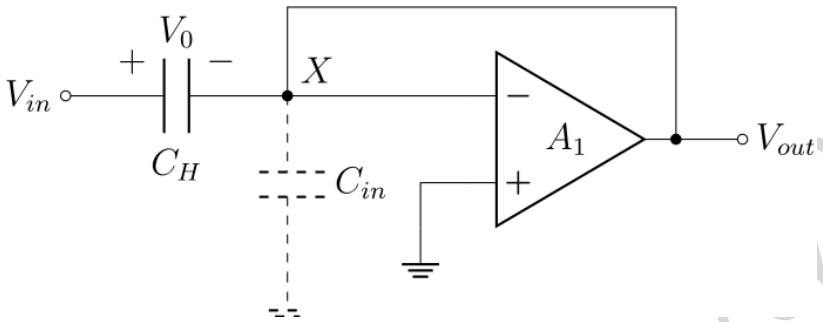

Figure 4: Question 5.(c)

UNIT - V

6 a) Determine the maximum INL for a 3-bit DAC with $V_{REF} = 5$ V which has the following characteristics. Does the DAC have 3-bit accuracy? **07**

Digital Input	Voltage Output (V)
000	0
001	0.625
010	1.562
011	2.000
100	2.500
101	3.125
110	3.438
111	4.375

b) Explain the construction and working of charge-scaling DACs. **09**

c) Given $V_{in} = 2.49$ V and $V_{REF} = 5$ V for a 4-bit successive approximation ADC. The comparator makes the wrong decision for the MSB conversion because of its offset. What will be the final digital output of the ADC in this case? **04**

OR

7 a) Calculate DNL for each digital code of the converter whose transfer curve is given in Figure 5. Also state the main issue with this converter and find its maximum resolution. **06**

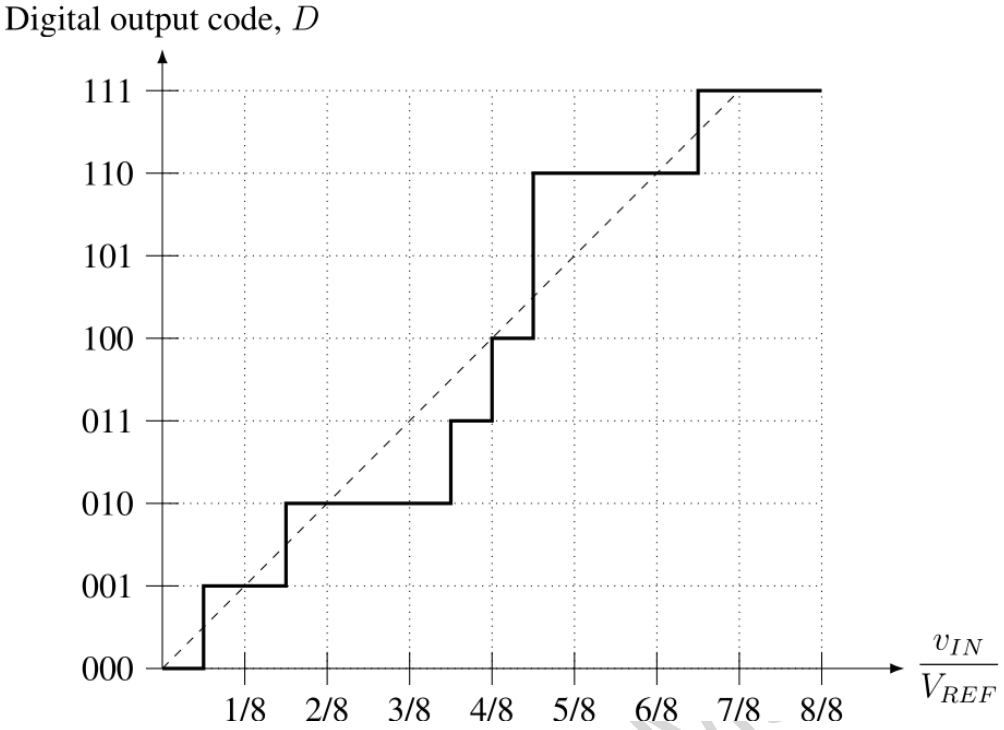

Figure 5: Question 7.(a)

b) Explain the working of a single slope integrating ADC with the help of block diagram and discuss the accuracy issues related to the same. **08**

c) With the help of a neat block diagram, find the output voltage for a 3-bit pipeline DAC for two cases: $D_A = 101$ and $D_B = 110$. Assuming $V_{REF} = 5$ V, find the total conversion time to perform both conversions. **06**

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