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B.M.S. College of Engineering, Bengaluru-560019

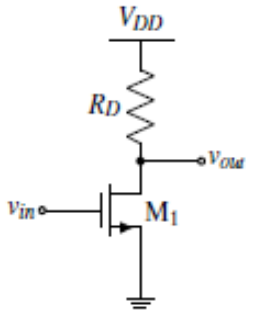
Autonomous Institute Affiliated to VTU

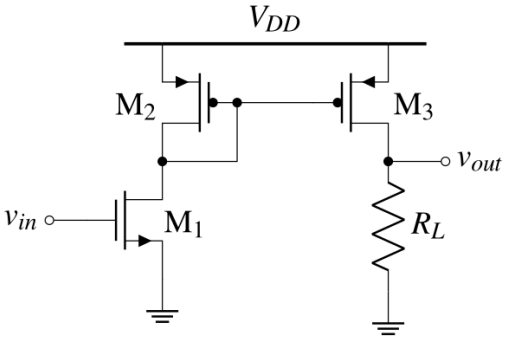
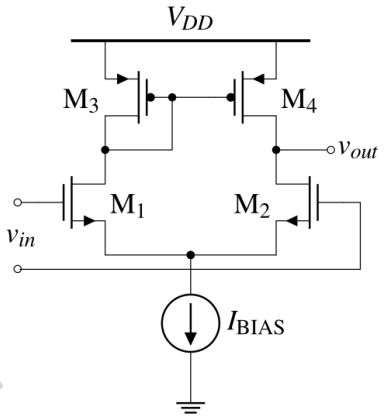
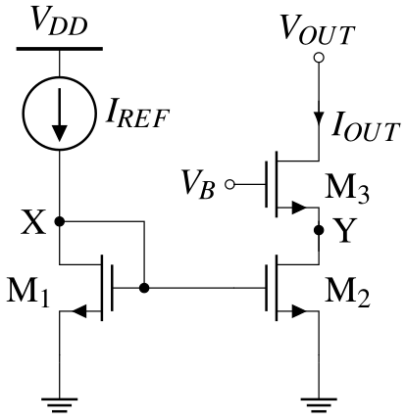
January / February 2025 Semester End Main Examinations

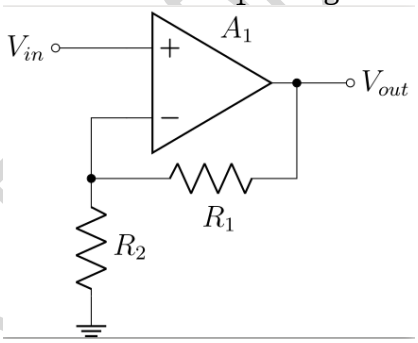
Programme: B.E. **Semester: VI**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC6PCMSD **Max Marks: 100**
Course: Mixed Signal Design

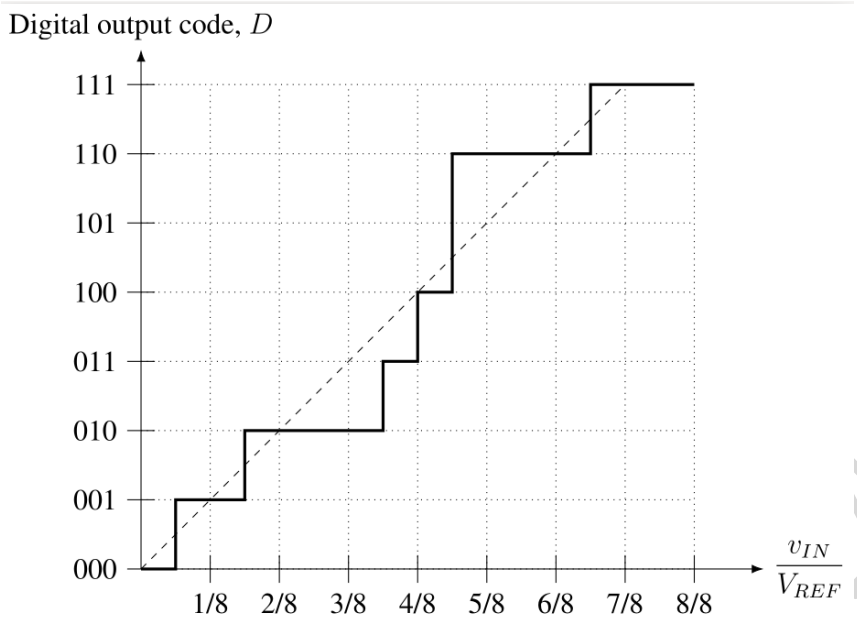
Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			CO	PO	Marks
		UNIT – I			
1	a)	Analyze the circuit shown in Figure 1 and determine the input voltage places M_1 at the edge of triode region, given (W/L) = 50/0.5, $R_D = 2k\Omega, \lambda = 0, \mu_n C_{ox} = 135\mu\ A/V^2$, $V_T = 0.7$ V and $V_{DD} = 3$ V. What is the output voltage under this condition?  Figure 1: Question 1(a)	CO2	PO2	10
	b)	Perform the quantitative analysis of a differential pair circuit and calculate the differential output current. Also, indicate the differential input voltage where the circuit transconductance falls to zero.	CO2	PO2	10
		OR			
2	a)	Analyze a source follower with resistive load and obtain an expression for the small-signal voltage gain. Also, illustrate its operation and mention its applications.	CO2	PO2	10
	b)	Perform the qualitative analysis of a differential pair circuit with the aid of input output characteristics plots. Illustrate that the small-signal gain is maximum for equal inputs.	CO2	PO2	10
		UNIT – II			
3	a)	With the help of neat circuit diagrams, justify the need for cascode current mirrors in integrated circuits.	CO1	PO1	05

		b)	With the help of neat circuit diagram and appropriate analyses, obtain the small-signal differential gain of a differential pair with current mirror load.	**CO2**	**PO2**	**10**
		c)	Find the small-signal voltage gain of the circuit shown in Figure 2.  Figure 2: Question 3(c)	**CO1**	**PO1**	**05**
			OR			
	4	a)	In the circuit shown in Figure 3, given I_{BIAS} = 100 µA, $(W/L)_{1-4}$ = 100/1, $\mu_n C_{ox}$ = 92 µA/V^2, V_T = 0.7 V and $\lambda_n = \lambda_p$ = 0.05/V, find the small-signal differential voltage gain.  Figure 3: Question 4(a)	**CO1**	**PO1**	**05**
		b)	Analyze the circuit shown in Figure 4 and demonstrate how the bias voltage V_B can be generated. Also, suggest a suitable modification to the circuit to increase the output voltage swing.  Figure 4: Question 4(b)	**CO2**	**PO2**	**10**
		c)	Determine the small-signal gain of a 5-transistor OTA in common-mode.	**CO1**	**PO1**	**05**

			UNIT - III			
	5	a)	Design a telescopic cascode op-amp to satisfy the following specifications: V_{DD} = 3 V, differential output swing = 3 V, power dissipation = 10 mW, voltage gain = 1000. Assume $\mu_n C_{ox}$ = 60 µA/V^2, $\mu_p C_{ox}$ = 30 µA/V^2 , λ_n = 0.1 V^{-1}, λ_p = 0.2 V^{-1} (for an effective channel length of 0.5 µm), γ = 0, $V_{THN} = \lvert V_{THP} \rvert$ = 0.7 V.	**CO3**	**PO3**	**10**
		b)	A single pole Op-Amp of DC gain 2000 and unity-gain bandwidth 10 Grad/s is used to realize a non-inverting amplifier of gain 5. For a step input, calculate the time needed for the output to reach within 2% of its final value.	**CO1**	**PO1**	**05**
		c)	With the help of a neat circuit diagram, demonstrate how the gain of a telescopic cascode Op-Amp can be enhanced by the technique of gain boosting. (Small-signal analysis not needed)	**CO1**	**PO1**	**05**
			OR			
	6	a)	Design a folded-cascode op-amp with an NMOS input pair to satisfy the following specifications: V_{DD} = 3 V, differential output swing = 3 V, power dissipation = 10 mW, voltage gain = 1000. Assume $\mu_n C_{ox}$ = 60 µA/V^2, $\mu_p C_{ox}$ = 30 µA/V^2 , λ_n = 0.1 V^{-1}, λ_p = 0.1 V^{-1} (for an effective channel length of 1 µm), γ = 0, $V_{THN} = \lvert V_{THP} \rvert$ = 0.7 V.	**CO3**	**PO3**	**10**
		b)	The circuit shown in Figure 5 is designed for a nominal gain of 20. Determine the minimum value of A_1 for a gain error of 0.5%.  Figure 5: Question 6(b)	**CO1**	**PO1**	**05**
		c)	Justify how a two-stage op-amp can overcome the gain and output swing limitation encountered by a telescopic cascode op-amp.	**CO1**	**PO1**	**05**
			UNIT – IV			
	7	a)	Demonstrate that the thermal noise sampled onto a capacitor is independent of the ON-resistance of the switch used to sample the input.	**CO1**	**PO1**	**05**

		b)	Calculate DNL for each digital code of the converter whose transfer curve is given in Figure 6. Also state the main issue with this converter and find its maximum resolution.  Figure 6: Question 7(b)	**CO1**	**PO1**	**05**
		c)	"By using separate pads and pins, the analog and the digital circuits are completely decoupled." Justify the statement with relevance to mixed signal layout issues.	**CO1**	**PO1**	**10**
			OR			
	8	a)	Demonstrate that a switched-capacitor can lead to the realization of a large resistance on-chip. Also highlight the limitations of such a realization.	**CO1**	**PO1**	**07**
		b)	Identify the various errors that can occur during the sample-and-hold process and describe them briefly, with the help of neat diagrams.	**CO1**	**PO1**	**08**
		c)	Determine the maximum INL for a 2-bit DAC with VREF = 5 V, which has the following characteristics. Does the DAC have 2-bit accuracy? Digital Input | Voltage Output (V) 00 | 0 01 | 1.75 10 | 2.75 11 | 3.75	**CO1**	**PO1**	**05**
			UNIT – V			
	9	a)	Design a 4-bit charge-scaling DAC using a split capacitor array. Determine the output voltage of the DAC for input digital codewords: (i) 1100 and (ii) 0011.	**CO3**	**PO3**	**08**
		b)	Given V_{in} = 2.49 V and V_{REF} = 5 V for a 4-bit successive approximation ADC. The comparator makes the wrong decision for the MSB conversion because of its offset. What will be the final digital output of the ADC in this case?	**CO1**	**PO1**	**05**

		c)	Explain the working of a single slope integrating ADC with the help of block diagram and discuss the accuracy issues related to the same.	-	-	**07**
			OR			
	10	a)	Design a 4-bit DAC using R-2R architecture with R = 1 kΩ, R_F = 2 kΩ and V_{REF} = 5 V. Assume that the resistances of the switches are negligible. Determine the output voltages for input digital codewords: (i) 1010 and (ii) 0101.	**CO3**	**PO3**	**08**
		b)	Demonstrate the application of the principle of binary search in converting an analog input of 3 V into 4-bit digital output codeword with V_{REF} = 5 V.	**CO1**	**PO1**	**05**
		c)	With the help of a neat block diagram, explain the working of a 3-bit pipeline ADC.	-	-	**07**

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