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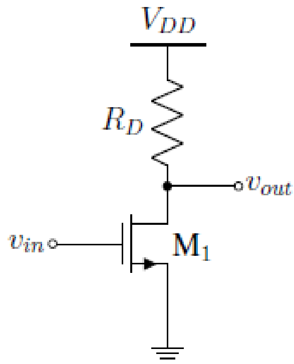
B.M.S. College of Engineering, Bengaluru-560019

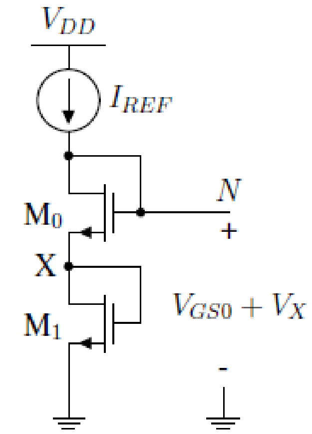
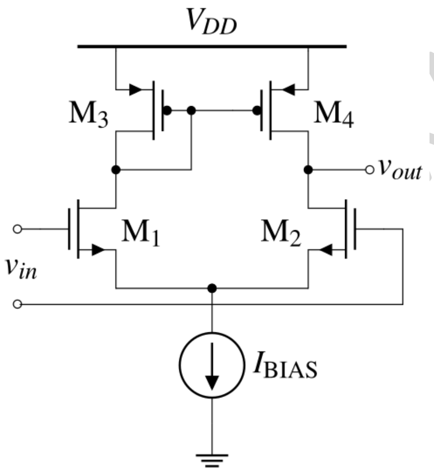
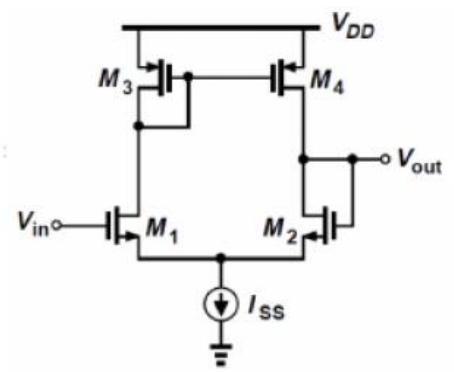
Autonomous Institute Affiliated to VTU

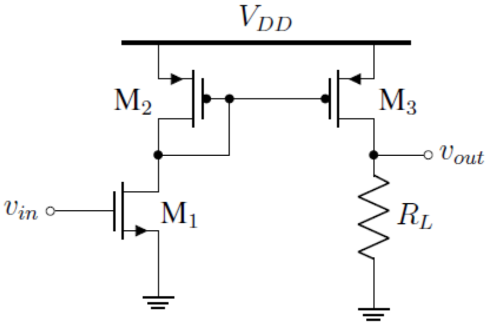
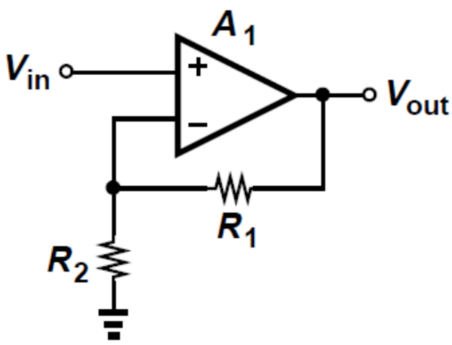
October 2024 Supplementary Examinations

Programme: B.E. | **Semester: VI**
Branch: Electronics and Communication Engineering | **Duration: 3 hrs.**
Course Code: 22EC6PCMSD | **Max Marks: 100**
Course: Mixed Signal Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			CO	PO	Marks
		UNIT – I			
1	a)	Perform the qualitative analysis of a differential pair circuit with the aid of input output characteristics plots. Demonstrate that the small-signal gain is maximum for equal inputs.	**CO2**	**PO2**	**10**
	b)	Analyze the circuit shown in Figure 1, given (W/L) = 50/0.5, R_D = 2 kΩ, λ= 0, μ_nC_{ox} = 1.34225 x10^{-4} A/V^2, V_T = 0.7 V, V_{DD} = 3 V. (i) What is the small signal gain if M_1 is in saturation and I_D = 1 mA? (ii) What input voltage places M_1 at the edge of triode region? What is the small-signal gain under this condition?  Figure 1: Question 1.(b)	**CO2**	**PO2**	**10**
		UNIT – II			
2	a)	Derive an expression for the small-signal differential gain of an operational transconductance amplifier.	**CO1**	**PO1**	**10**

		b)	Modify the circuit shown in Figure 2 to construct a Cascode current mirror. Analyze the circuit thus obtained and demonstrate that one threshold voltage is wasted in voltage headroom.  Figure 2: Question 2.(b)	**CO**2	**PO2**	**05**
		c)	For the circuit shown in Figure 3, given I_{BIAS} = 100µA, $(W/L)_{1\text{-}4}$ = 100/1, $\mu_n C_{ox}$ = 92 µA/V^2, V_T = 0.7 V and $\lambda_n = \lambda_p$ = 0.05/V, find the small-signal differential voltage gain.  Figure 3: Question 2.(c)	**CO1**	**PO1**	**05**
			OR			
	3	a)	Calculate the input common-mode voltage range and the closed loop output impedance of the unity gain buffer shown below in Figure 4, given: threshold voltage of each device 0.7 V and overdrive voltage 0.3 V. Comment on the result.  Figure 4: Question 3.(a)	**CO**1	**PO1**	**10**

	b)	Determine the small-signal voltage gain of the circuit shown in Figure 5.  Figure 5: Question 3.(b)	**CO**1	**PO1**	**05**
	c)	Analyze the large signal behavior of an OTA using 5 transistor realization.	**CO2**	**PO2**	**05**
		UNIT - III			
4	a)	Design a fully differential telescopic Op Amp with the following specifications: V_{DD}=3V, differential output swing = 3 V, power dissipation = 9mW, Voltage gain = 1200. Assume $\mu_n C_{ox}$ = 60 $\mu A/V^2$, $\mu_p C_{ox}$ = 30 $\mu A/V^2$, λ_n = 0.1 V^{-1}, λ_p = 0.2 V^{-1} (for an effective channel length of 0.5 µm), γ=0 and V_{THN} =|V_{THP}|=0.6V.	**CO**3	**PO3**	**10**
	b)	Bring out the importance of the following performance parameters of Op-Amp in the context of system design: (i) Gain (ii) Output swing (iii) Noise and offset (iv) Linearity (v) Small-signal bandwidth.	**CO**1	**PO1**	**10**
		OR			
5	a)	The circuit shown in the Figure 6 is designed for a nominal gain of 10, i.e., $(1 + R_1/R_2) = 10$. Determine the minimum value of A_1 for a gain error of 1%. Also determine the time taken for the output to settle to within 2% of its final value given the unity gain bandwidth of the OpAmp to be 3×10^9 rad/s.  Figure 6: Figure 5.(a)	**CO**1	**PO1**	**10**
	b)	Design a two stage op-amp whose first stage is a telescopic cascode stage. Justify that the swing limitation of the telescopic cascode structure is thus overcome.	**CO**3	**PO3**	**10**

			UNIT – IV			
	6	a)	Design a non-inverting amplifier using switched capacitors.	**CO**3	**PO3**	**10**
		b)	Determine the maximum DNL (in LSBs) for a 3-bit DAC, which has the characteristics as given in Table 1. Does the DAC have 3-bit accuracy? If not, what is the resolution of the DAC having this characteristic?	**CO1**	**PO1**	**10**
			UNIT – V			
	7	a)	Determine the output digital code for a 3 bit pipeline ADC for inputs of 2 V, 3 V and 4.5V. Assume V_{REF}=5 V. What is the total time taken for the said conversion?	**CO1**	**PO1**	**10**
		b)	Design a 3-bit charge-scaling DAC and find the value of the output voltage for i) $D_2D_1D_0$ = 010 and ii) $D_2D_1D_0$ = 101. Assume that V_{REF}= 5 V and C= 0.5 pF.	**CO**3	**PO3**	**10**

Table 1: Question 6.(b)

Digital Input	**Voltage Output**
000	0 V
001	0.620 V
010	1.560 V
011	2.000 V
100	2.500 V
101	3.130 V
110	3.430 V
111	4.375 V

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