U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**

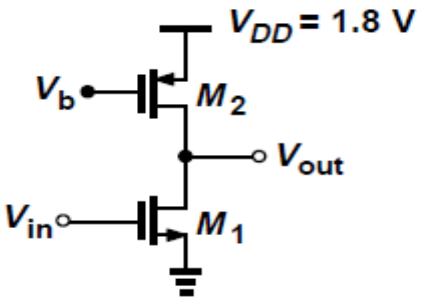
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**

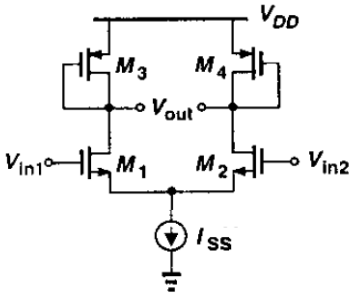
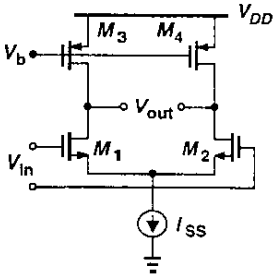
Course Code: 23EC6PCMSD / 22EC6PCMSD **Max Marks: 100**

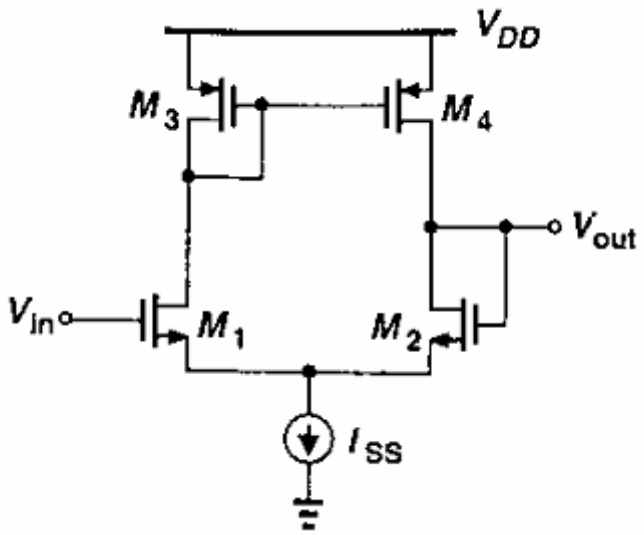
Course: MIXED SIGNAL DESIGN

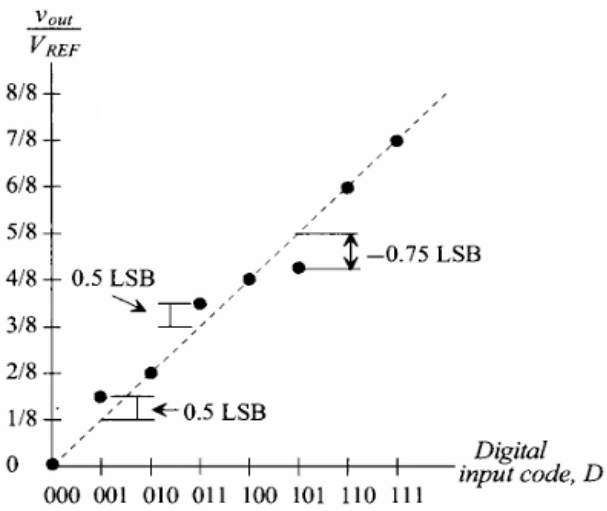
Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	It was observed that a MOSFET acted as a resistor when its gate and drain were shorted. (i) Identify the configuration and draw the circuit, small signal model. (ii) Justify how the input-output characteristic is relatively linear for this connection with all necessary equations.	*1*	*1*	**10**
	b)	Plot the input-output characteristic of a differential pair as the device width and tail current vary.	*1*	*1*	**10**
		OR			
2	a)	Deduce an expression for G_m, R_{out} and A_v of a Cascode stage amplifier.	*1*	*1*	**10**
	b)	The Common source stage of Fig 2b must provide a voltage gain of 10 with a bias current of 0.5mA. Assume $\lambda_1 = 0.1V^{-1}$ and $\lambda_2 = 0.15V^{-1}$, Kp' = 100μA/V^2 and Kn' = 200μA/V^2 (a) Compute the required value of $(W/L)_1$. (b) if $(W/L)_2 = 20/0.18$, calculate the required value of V_B.  Fig 2b	*1*	*1*	**10**

			UNIT - II			
	3	a)	Draw basic current mirror circuit, analyze the working and illustrate that the current at output is independent of process and temperature.	*2*	*2*	**10**
		b)	For the differential pairs shown In Fig 3b find Differential gain and Minimum allowable input common mode range such that I_{SS} maintains 0.5V across it. Use the data given Kn` 60μA/V$^2$ Kp` 30μA/V^2 (W/L)n 100 (W/L)p 50 Vtn 0.7V Vtp -0.7V λn 0.1V^{-1} λp 0.2V^{-1} Vdd 3V  Fig 3b	*1*	*1*	**10**
			OR			
	4	a)	Show the qualitative analysis of a differential pair circuit with the help of input output characteristics plots. Illustrate that small-signal gain is maximum for equal inputs.	*2*	*2*	**10**
		b)	In the circuit shown in Fig 4b, $(W/L)_{1-4}$ =50/0.5, μ_pC_{ox}=38.36 μA/V^2, μ_nC_{ox}=134.2 μA/V^2, V_{thn}=0.7V, V_{thp}=-0.8V and I_{SS}=1mA. (i) What is the small signal differential gain? (ii) For $V_{in(CM)}$=1.5V, what is the maximum allowable output voltage swing?  Fig 4b	*1*	*1*	**10**
			UNIT - III			
	5	a)	With transistor level implementation, describe amplifier gain boosting. Modify the arrangement to obtain regulated cascade structure and illustrate how gain boosting is applicable to both signal path and load devices in case of telescopic OPAMP and folded cascade OPAMP.	*1*	*1*	**10**
		b)	Highlight the significance of two stage OPAMP and draw the following circuits and write the gain expression: (i) Simple two stage OPAMP (ii) Two stage OPAMP employing cascading	*1*	*1*	**10**

			OR			
	6	a)	Discuss the importance of each of the following OPAMP design parameters: (i) Gain (ii) Small signal bandwidth (iii) Large signal bandwidth (iv) Output swing (v) Linearity	*1*	*1*	**10**
		b)	Calculate the input common mode voltage range and the closed loop output impedance of the unity gain buffer shown in Fig 6b  Fig 6b	*1*	*1*	**10**
			UNIT - IV			
	7	a)	Determine the DNL and INL for a 3-bit DAC with the following characteristics (Table 7a) Digital Input — Voltage Output (V) 000 — 0 001 — 0.625 010 — 1.5625 011 — 2 100 — 2.5 101 — 3.125 110 — 3.4375 111 — 4.375 Table 7a	*1*	*1*	**10**
		b)	Highlight the significance of the following in addressing the mixed signal design issues: i) Power supply and grounding ii) Floor planning	*1*	*1*	**10**
			OR			

	8	a)	With the help of relavant equations and diagrams illustrate the working of Switched capacitors as MOSFETS.	*1*	*1*	**10**
		b)	Determine the INL for the nonideal 3-bit DAC shown in Fig. 8b. Assume that Vref=5V. Also show the INL plot for the same.  Fig 8b	*1*	*1*	**10**
			UNIT - V			
	9	a)	Design a 3-bit DAC using R-2R architecture with R = 1KΩ; R_F = 2KΩ and V_{REF} = 5V . Determine I_{TOT} for each digital input and corresponding output voltage, Vout.	*3*	*3*	**10**
		b)	List the merits and demerits of pipelined ADC and show the conversion process for (a) Vin = 2V (b) Vin = 4V (c) Vin = 5.5V. Assume Vref = 5V and N=3.	*1*	*1*	**10**
			OR			
	10	a)	With a neat block diagram, describe the principle of a successive approximation ADC. Illustrate the conversion process for analog voltage of 6.1 V.	*1*	*1*	**10**
		b)	With neat circuit diagram describe charge scaling DAC. Also highlight the significance of centroid capacitance in designing the charge scaling circuits.	*3*	*3*	**10**

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