U.S.N.										

B. M. S. College of Engineering, Bengaluru - 560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: VII**
Branch: ES – Cluster Elective **Duration: 3 hrs.**
Course Code: 19EC7CE2LV **Max Marks: 100**
Course: Low Power VLSI **Date: 12.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1. a) Describe the CMOS N-Well process with neat diagrams. **12**

   b) Discuss the following short channel effects and its impact on the device performance: i) Channel length modulation ii) Drain Induced barrier Lowering. **08**

UNIT - II

2. a) What is Pass transistor Logic? Realize a 4x1 Mux using Pass Transistor Logic. **08**

   b) What is short circuit power dissipation? Obtain an expression for Short circuit power dissipation in an Inverter cell. **12**

UNIT - III

3. a) Compare Constant Field scaling versus Constant Voltage scaling effects on the key device parameters. **10**

   b) With the help of 16-bit adder architecture, discuss parallelism for low power. **10**

UNIT - IV

4. a) What is clock gating? Discuss with neat diagrams. **08**

   b) What is Dynamic CMOS Logic? Discuss its Advantages and Disadvantages. **12**

OR

5. a) Discuss the VTCMOS approach for subthreshold leakage current reduction. **10**

   b) What is Power gating? Compare clock gating and power gating. **10**

UNIT - V

6.	a)	Discuss the Adiabatic charging of a capacitor with neat diagrams.	**10**
	b)	Briefly discuss Battery aware system design.	**10**

OR

7.	a)	What are the Machine independent software optimizations? Discuss.	**10**
	b)	Discuss Energy aware routing with neat diagrams.	**10**

*****