U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

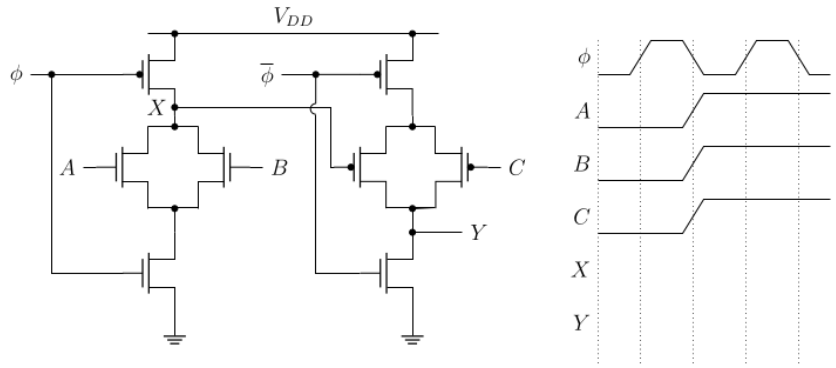
Autonomous Institute Affiliated to VTU

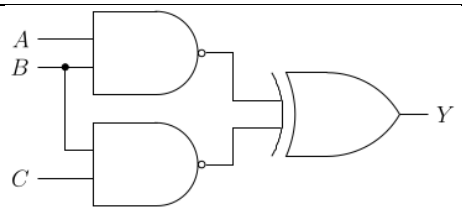
January 2024 Semester End Main Examinations

Programme: B.E. **Semester: VII**
Branch: ES – Cluster Elective **Duration: 3 hrs.**
Course Code: 19EC7CE2LV **Max Marks: 100**
Course: Low Power VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Analyze the problem of latch-up in the CMOS fabrication and mention any one technique of avoiding it.	CO2	PO2	06
	b)		Analyze the DC characteristics of a Static CMOS inverter and obtain expressions for V_{IH} and V_{IL}.	CO2	PO2	10
	c)		Briefly describe any one technique of driving large capacitive loads.	--	--	04
			UNIT - II			
2	a)		Analyze the circuit shown in Figure 1 and determine the Boolean function (Y) that is implemented. Also, complete the waveform shown alongside the circuit.  Figure 1: Question 2.(a)	CO2	PO2	06
	b)		Assuming that the inputs A, B and C of the circuit shown in Figure 2 are mutually independent and each take values '0' and '1' with equal probability, analyze and obtain the probability of the output Y switching from '0' to '1'.	CO2	PO2	06

			 Figure 2: Question 2.(b)			
		c)	Design circuits to implement the Boolean function $Y = B + \overline{A} \cdot \overline{C}$ in the following circuit styles: (i) Pass-Transistor Logic (ii) Dynamic CMOS	***CO3***	***PO3***	**08**
			UNIT - III			
	3	a)	Compare and contrast constant-field scaling and constant-voltage scaling.	***CO1***	***PO1***	**07**
		b)	Illustrate the means of achieving low power consumption by combining the techniques of pipelining and parallelism, without compromising on the performance of a suitable circuit.	***CO1***	***PO1***	**09**
		c)	Analyze and estimate the maximum energy savings possible for a microprocessor when its workload drops to 50% of the peak workload.	***CO2***	***PO2***	**04**
			UNIT - IV			
	4	a)	The sample of data to be sent on an 8-bit data bus is given below: {11111111, 10010000, 10001001, 00001111} Apply the concept of bus encoding technique to minimize the power consumption. Hence suggest the appropriate encoding scheme. Draw the circuit that can be used for encoding and decoding and show the encoding of data at each step.	***CO1***	***PO1***	**10**
		b)	Briefly discuss the various sources of power dissipation in CMOS integrated circuits.	***CO1***	***PO1***	**10**
			OR			
	5	a)	Give a scheme for the reduction of leakage power dissipation using dual-V_t approach without compromise in performance. Compare its performance with the MTCMOS approach.	***CO1***	***PO1***	**10**
		b)	Describe the transistor stack effect and demonstrate its application in reducing leakage power dissipation.	***CO1***	***PO1***	**10**
			UNIT - V			
	6	a)	Demonstrate that the charging of a capacitor C in n steps to a voltage V_{DD} instead of a conventional single-step charging reduces the energy consumption by a factor of n. Discuss the disadvantages of step-wise driver circuits for charging capacitive loads.	***CO1***	***PO1***	**10**
		b)	Discuss the working of an adiabatic amplifier with the help of a neat circuit diagram.	--	--	**10**
			OR			

	7	a)	Determine the constraints to be adhered to while scheduling tasks with voltage scaling. Also describe any two approaches of task scheduling with voltage scaling in battery driven systems.	***CO1***	***PO1***	**10**
		b)	Briefly discuss any three techniques of compiling code for low power with suitable examples.	--	--	**10**

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