U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: VII**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC7CE2LV **Max Marks: 100**
Course: Low Power VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Analyze the Latch-up problem in CMOS technology and demonstrate any two techniques to prevent it.	CO2	PO2	07
	b)	Illustrate the following: - i. Advantages of Silicon on Insulator (SOI) over CMOS technology ii. Effect of Drain Induced Barrier Lowering (DIBL) on the leakage current of MOS transistors	CO1	PO1	06
	c)	Compare the performance of the different types of inverters with respect to noise margins, power consumption and output voltage.	CO2	PO2	07
		OR			
2	a)	Analyse and justify that the sizing of PMOS devices are almost twice that of NMOS devices in a symmetric CMOS inverter.	CO2	PO2	07
	b)	Illustrate, with the help of a neat diagram, that the FinFET device is better suited for low power operation compared to planar CMOS devices.	CO1	PO1	06
	c)	Justify that a cascaded stage of inverters of increasing size minimizes the overall delay while driving a large capacitive load. Hence obtain the optimal relative dimension of two consecutive stages.	CO2	PO2	07
		UNIT - II			
3	a)	Demonstrate the contribution of the following to leakage power dissipation: i. P-N Junction Reverse-Biased Current ii. Subthreshold Leakage Current	CO1	PO1	06
	b)	Design the pass-transistor realization of the Boolean function $f = \overline{a}b + a\overline{b}$ using the minimum number of transistors. List the advantages and disadvantages of the pass transistor logic.	CO3	PO3	07
	c)	Design circuits to realize the Boolean function $f = x_3(x_1 + x_2)$ using the following circuit styles:	CO3	PO3	07

			i. Static CMOS ii. Dynamic CMOS			
			OR			
	4	a)	A 32 bit off-chip bus operating at 4.8 Volt and 64 MHz clock rate is driving a capacitance of 25 pF/bit. Each bit is estimated to have toggling probability of 0.25 at each clock cycle. What is the power dissipation operating the bus?	***CO1***	***PO1***	**05**
		b)	Design a 3-input dynamic NAND gate and illustrate the additional power dissipation due to the phenomenon of charge sharing.	***CO3***	***PO3***	**07**
		c)	Design circuits to realize the Boolean function $Y = \bar{s}A + sB$ in the following styles: (i) Pass-Transistor Logic (ii) Complementary Pass-Transistor Logic (iii) Static CMOS	***CO3***	***PO3***	**08**
			UNIT - III			
	5	a)	Demonstrate the application of Dynamic Voltage and Frequency Scaling in reducing the dynamic power consumption.	***CO1***	***PO1***	**06**
		b)	Differentiate between Constant Voltage Scaling and Constant Field Scaling.	***CO2***	***PO2***	**06**
		c)	Illustrate the application of Parallelism and Pipelining in achieving lower power consumption.	***CO1***	***PO1***	**08**
			OR			
	6	a)	Demonstrate how the energy consumed by a microprocessor can be reduced by 75% when its workload drops to 50% of the peak workload.	***CO1***	***PO1***	**06**
		b)	Analyze the effects of reduction in power supply voltage on the speed and other performance parameters of the CMOS circuit.	***CO2***	***PO2***	**06**
		c)	Demonstrate how loop unrolling can help reduce power consumption by taking the example of an IIR filter given by $y_n = x_n + k \times y_{n-1}$.	***CO1***	***PO1***	**08**
			UNIT - IV			
	7	a)	Discuss the application of Dual-V_t Assignment Approach (DTCMOS) to reduce leakage power.	***CO1***	***PO1***	**08**
		b)	Describe the different topologies of power gating.	--	--	**06**
		c)	Justify how the technique of clock gating reduces power consumption.	***CO2***	***PO2***	**06**
			OR			
	8	a)	Discuss the realization of Gated Clock FSM, with relevant diagrams, to reduce dynamic power.	***CO1***	***PO1***	**08**
		b)	Analyze the cases where glitching power arises, and suggest techniques to minimize it.	***CO2***	***PO2***	**06**
		c)	Describe the advantages and disadvantages of the following logic styles with respect to power, area and delay. i. Dynamic CMOS ii. Static CMOS	--	--	**06**

			UNIT - V			
	9	a)	Design a 2-input AND/NAND gate using the concept of adiabatic circuits, describing its operation in detail.	***CO3***	***PO3***	**10**
		b)	Discuss, with the help of neat diagrams, the importance of pulsed power supplies in adiabatic circuits.	*--*	*--*	**10**
			OR			
	10	a)	Design a 2-input OR/NOR gate using the concept of adiabatic circuits, describing its operation in detail.	***CO3***	***PO3***	**10**
		c)	Discuss the concept of energy aware routing and bring out its importance.	*--*	*--*	**10**

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