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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: VII**
Branch: Institutional Elective **Duration: 3 hrs.**
Course Code: 19EC7OE2MC **Max Marks: 100**
Course: Fundamentals of Mobile Communications

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Draw the network architecture of cellular system and mention its important entities.	CO1	PO1	10
	b)	Explain features of cordless and paging system	CO1	PO1	10
		UNIT - II			
2	a)	If a total of 33 MHz of bandwidth is allocated to a particular FDD cellular system which uses 25 kHz pairs, compute the number of channels available per cell if a system uses i. 4 cell reuse ii. 7 cell reuse iii. 12 cell reuse If 1 MHz is allocated for control channels, determine a distribution of control and voice channels	CO1	PO1	10
	b)	Differentiate the following with respect to mobile communication system: i. Co-channel interference ii. Adjacent channel interference.	CO1	PO1	10
		UNIT - III			
3	a)	Explain inter BSC hand over procedure in GSM.	CO1	PO1	10
	b)	Classify the channels for communication in GSM system.	CO1	PO1	10
		OR			
4	a)	Analyse the GSM frame structure with necessary diagrams.	CO1	PO1	10
	b)	Identify the steps involved in handoff if MS is moving from MSC A to MSC B.	CO1	PO1	10

			UNIT - IV			
	5	a)	Write the features of entities in Mobile IP and explain how packet is directed in mobile IP architecture from home agent when Mobile node moves away from home network.	***CO1***	***PO1***	**10**
		b)	Compare Bluetooth with UWB technology and list the applications of UWB.	***CO1***	***PO1***	**10**
			OR			
	6	a)	Explain the UMTS architecture and functionalities of packet switched elements.	***CO1***	***PO1***	**10**
		b)	Indicate the network components of WLAN system and their functionalities and list any two applications of WLAN.	***CO1***	***PO1***	**10**
			UNIT - V			
	7	a)	List values added attributes of m-commerce and explain functionalities of user plane and service provider plane defined in m-commerce frame work.	***CO2***	***PO4***	**10**
		b)	Discuss the classification of m-commerce class of applications and emerging applications.	***CO2***	***PO4***	**10**

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April 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: VII**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC7PCESD **Max Marks: 100**
Course: Embedded System Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Compare Harvard V/s Von-Neumann Processor/Controller Architecture with a neat diagram.	CO2	PO2	6
	b)	What is the Significance of "Watchdog Timer" in Embedded Systems? For a watchdog timer working on 4 kHz clock and timeout time of 500ms , calculate the value of the counter.	CO1	PO1	7
	c)	Discuss the Operational and Non-operational quality attributes of embedded systems. Which Quality attribute describes the new firmware or hardware technology?	CO2	PO2	7
		UNIT - II			
2	a)	'SPI bus is most suitable for application requiring transfer of data in 'streams''. Justify with neat diagrams.	CO1	PO1	10
	b)	With the workflow design of a DMA controller analyze when an input device sends a DMA request. Why DMA is preferred than interrupt for faster and bulk data transfer?	CO3	PO3	10
		OR			
3	a)	Discus the three common cache replacement policies. Given a 2-level cache design where the hit rates are 88% for the smaller cache and 97% for the larger cache, the access costs for a miss are 12 cycles and 20 cycles, respectively, and the access cost for a hit is one cycle, calculate the average cost of access.	CO1	PO1	10
	b)	Design 32X4 RAM module using 8X4 RAM chips. Assume processor is having 7 address line. The range of address to be used is 60 to 7F .	CO3	PO3	10
		UNIT - III			
4	a)	Develop an embedded C code to interface LPC 1768 Microcontroller with a relay switch to the control Buzzer.	CO3	PO3	10

		b)	Analyse the different embedded firmware design approaches. With an example, discuss in detail the Super Loop approach with Pros, Cons and Enhancements.	***CO2***	***PO2***	**10**
			OR			
	5	a)	Discuss the advantage and limitations/drawbacks of Assembly language based embedded firmware development. What is the benefit of 'library file'?	***CO2***	***PO2***	**8**
		b)	Develop a device driver pseudocodes for communication over I2C bus.	***CO3***	***PO3***	**8**
		c)	Compare Compiler and Cross-Compiler.	***CO2***	***PO2***	**4**
			UNIT - IV			
	6	a)	Compare Round robin and priority based preemptive scheduling. Three processes with process IDs P1, P2, P3 with estimated completion time 6, 4, 2 milliseconds respectively, enters the ready queue together in the order P1, P2, P3. Calculate the waiting time and Turn Around Time (TAT) for each process and the Average waiting time and Turn Around Time (Assuming there is no I/O waiting for the processes) in preemptive scheduling RR algorithm with Time slice= 2ms.	***CO1***	***PO1***	**10**
		b)	Discuss the various Task synchronization issues using the Dining Philosophers problem.	***CO2***	***PO2***	**10**
			UNIT-V			
	7	a)	List and discuss the various techniques available for embedded firmware debugging.	***CO2***	***PO2***	**10**
		b)	Discuss in detail the types of files generated during cross-compilation of an Embedded C Code.	***CO1***	***PO1***	**10**

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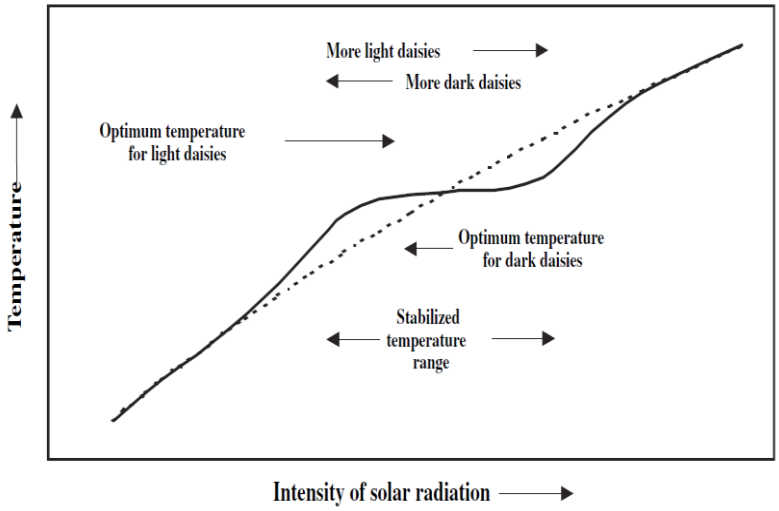
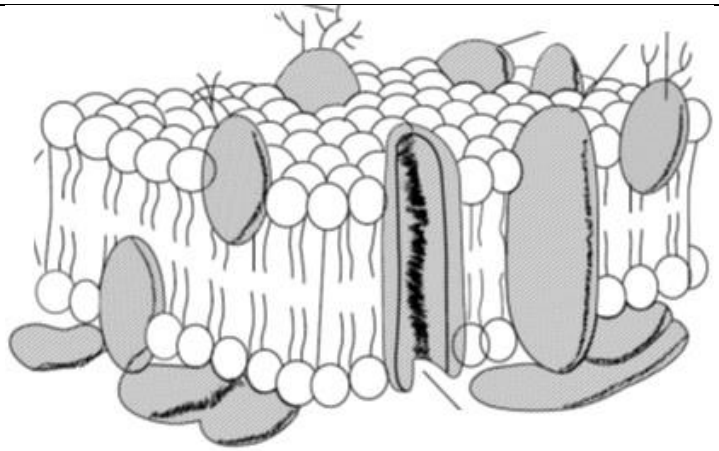
April 2024 Semester End Make-Up Examinations

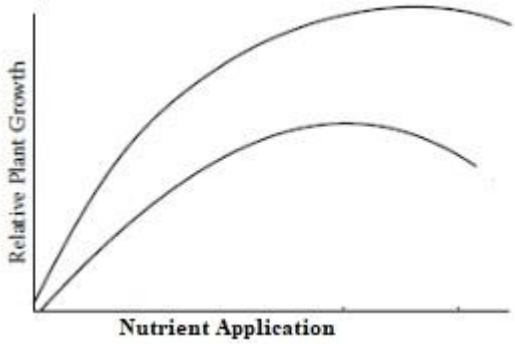
Programme: B.E. **Semester: VII**
Branch: ES Cluster (EEE/ET/ECE/EIE/MD) **Duration: 3 hrs.**
Course Code: 19ES7BSBFE **Max Marks: 100**
Course: BIOLOGY FOR ENGINEERS

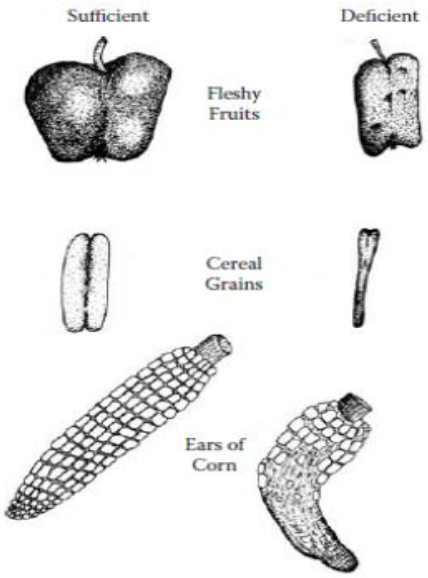
Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Define the term Life and also discuss its characteristics.	*CO1*	-	**06**
	b)	Analyze the concept of Genetic drift including analysis of the Bottleneck effect.	*CO2*	*PO1*	**07**
	c)	Consider the **Fig. 1** given below. Identify and analyze the hypothesis.  **Fig. 1**	*CO2*	*PO1*	**07**
		UNIT - II			
2	a)	Analyze the different Monosaccharides of carbohydrates and the Monosaccharide derivatives. Include any basic Monosaccharide structure in your analysis.	*CO2*	*PO1*	**10**
	b)	Considering the **Fig.2** given below; sketch and analyze its various parts and characteristics.	*CO2*	*PO1*	**10**

			 **Fig. 2**			
			OR			
	3	a)	Analyze the importance of Nucleic acids in living beings. Sketch the different nucleotide bases used in DNA and briefly analyze the importance of 'Double Helix' structure of DNA.	*CO2*	*PO1*	**10**
		b)	Considering the **Fig.3** given below, sketch and thereby analyze its various parts and characteristics.  **Fig. 3**	*CO2*	*PO1*	**10**
			UNIT - III			
	4	a)	Define the different types of radiation and also analyze the penetrating power of radiations on human body and the process of stopping the radiations.	*CO3*	*PO6*	**10**
		b)	With relevant diagram, analyze the generation of X-rays through an X-ray generator.	*CO3*	*PO6*	**10**

			UNIT - IV			
	5	a)	Explain the ionization effect due to radiation on human body and also analyze the effect of radiation on human DNA. Support your analysis with relevant diagrams.	*CO3*	*PO6*	**06**
		b)	Explain the two different classifications for In-vitro studies of the effects of RF fields. Also briefly explain the mutation analysis procedure.	*CO3*	*PO6*	**07**
		c)	Analyze the following effects of radiation: i. Deterministic effects ii. Stochastic effects	*CO3*	*PO6*	**07**
			UNIT - V			
	6	a)	Analyze the importance of Phosphorous in organic farming. Also analyze the effects of Phosphorous on plant growth and quality with relevant diagrams.	*CO4*	*PO7*	**10**
		b)	Identify the nutrient that follows the given graph in **Fig. 4** towards vegetative growth and reproductive growth when supplemented in different quantities. Analyze the process in detail and also identify the different growth processes in the graph.  **Fig. 4**	*CO4*	*PO7*	**10**
			OR			

	7	a)	The following **Fig. 5** depicts two phenomena when a particular nutrient was sufficient and deficient for plants. Identify the nutrient and analyze the causes for this symptom.  **Fig. 5**	*CO4*	*PO7*	**10**
		b)	The following phenomena was observed due to deficiency of a plant nutrient in **Fig. 6**. Identify the nutrient and analyze the causes for this symptom.  **Fig. 6**	*CO4*	*PO7*	**10**

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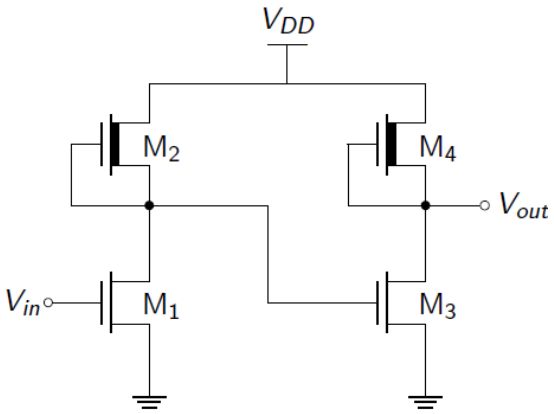
April 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: VII**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 19EC7CE2LV **Max Marks: 100**
Course: Low Power VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Analyze and obtain the DC characteristics of an inverter with Enhancement-mode nMOS as pull-up device.	CO2	PO2	7
	b)	Justify that a cascaded stage of inverters of increasing size minimizes the overall delay while driving a large capacitive load. Hence obtain the optimal relative dimension of two consecutive inverter stages.	CO2	PO2	5
	c)	Analyze the circuit shown in Figure 1 and obtain the aspect ratios of the transistors involved for the condition that the output of second inverter is equal to that of first inverter at V_{inv}, given V_{DD} = 3.3 V; inverter mid-point voltage, V_{inv} = 1.65 V; threshold voltage of NMOS transistor, $V_{t1} = V_{t3}$ = 0.5 V and threshold voltage of n-type depletion mode transistor, $V_{t2} = V_{t4} = -1.2$ V.  Figure 1: Question 1(c)	CO2	PO2	8
		UNIT - II			
2	a)	Design circuits to realize the Boolean function Y =A+$\bar{B}$.C in the following styles: i. Complementary Pass-Transistor Logic ii. Double Pass-Transistor Logic iii. Static CMOS	CO3	PO3	10

		b)	Design a 2×1 multiplexer using complementary pass-transistor logic (CPL) style circuit and discuss its working principle and functionality in detail.	***CO3***	***PO3***	**10**
			UNIT - III			
	3	a)	Briefly describe Adaptive Voltage Scaling with the help of a neat block diagram.	--	--	**10**
		b)	Justify how the following techniques could be used to reduce power consumption in VLSI Circuits and Systems without compromising on performance. i) Pipelining ii) Dynamic Voltage and Frequency Scaling	***CO2***	***PO2***	**10**
			UNIT - IV			
	4	a)	Demonstrate, with the help of a suitable example, the use of dual-V_t transistors in integrated circuits to minimize leakage power consumption without compromising on performance. Also briefly discuss any two techniques by which transistors of different threshold voltages can be realized on silicon.	***CO1***	***PO1***	**10**
		b)	The sample of data to be sent on an 8-bit data bus is given below: {11111111, 10010000, 10001001, 00001111} Analyze and suggest the proper bus encoding technique to minimize the power consumption. Draw the circuit that can be used for encoding and decoding. Hence show the encoding of data at each step.	***CO2***	***PO2***	**10**
			OR			
	5	a)	Demonstrate how the following techniques could be used to reduce power consumption in VLSI Circuits and Systems without compromising on performance. i) Clock gating ii) VTCMOS approach	***CO1***	***PO1***	**10**
		b)	Analyze how power-gating approach can be used to minimize leakage power dissipation and discuss any two power gating topologies.	***CO2***	***PO2***	**10**
			UNIT - V			
	6	a)	Design a 2-input OR/NOR Boolean functions using adiabatic realization and discuss its operation in detail.	***CO3***	***PO3***	**10**
		b)	Discuss the 2N and 2N2P logic styles for asynchronous power clock generators with the help of neat diagrams. What is the need for synchronous power clock generators?	--	--	**10**
			OR			
	7	a)	Design a 2-input AND/NAND gate using adiabatic realization and discuss its working principle in detail.	***CO3***	***PO3***	**10**
		b)	Discuss the working of an adiabatic amplifier with the help of neat diagrams.	--	--	**10**

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